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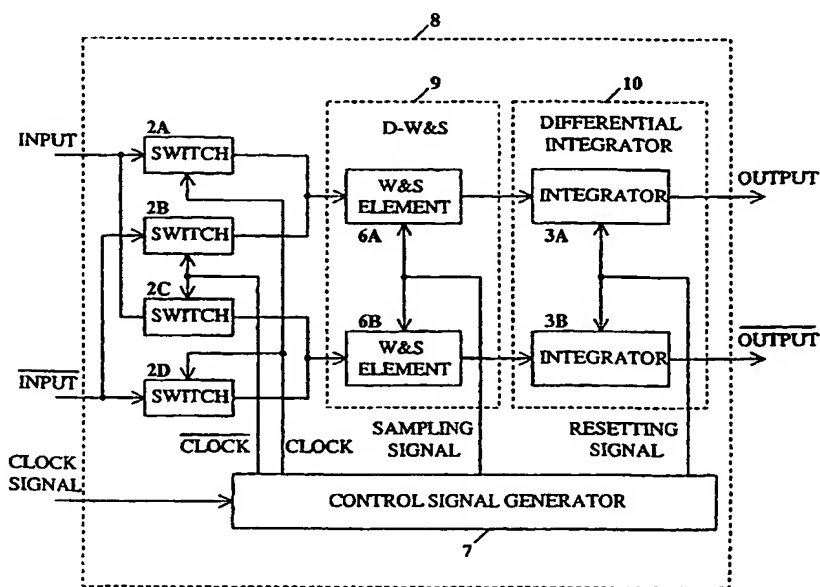
(57) Abstract: A charge sampling (CS) circuit (1), comprising a control signal generator (4) for controlling an analog input signal to the charge sampling circuit (1) to be integrated by an integrator (3) during a sampling phase responsive to a sampling signal from the control signal generator (4), wherein the current of the analog input signal is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output at the end of the sampling phase.

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TITLE: VERSATILE CHARGE SAMPLING CIRCUITS

BACKGROUND OF THE INVENTION

Voltage sampling is traditionally used for ana-log-to-digital (A/D) conversion. In a voltage sampler, a sampling switch is placed between a signal source and a capacitor. Between two sampling moments, the capacitor voltage tracks the signal voltage accurately. At the sampling moment, the switch is turned off to hold the capacitor voltage. The two processes become increasingly difficult when the signal frequency increases. For a given accuracy, thermal noise and switching noise set a minimum allowable capacitance while the tracking speed set a maximum allowable capacitance or switch resistance. It becomes impossible when the maximum is smaller than the minimum. Moreover, the clock jitter and finite turning-off speed (nonzero sampling aperture) make the sampling timing inaccurate. In fact, the bandwidth of a voltage sampling circuit must be much larger than the signal bandwidth. This makes direct sampling of high frequency radio signal extremely difficult. Sub-sampling can reduce the sampling rate but not the bandwidth of sampling circuit and not the demands on small clock jitter and small sampling aperture.

SUMMARY OF THE INVENTION

The object of the invention is to provide an improved sampling circuit and a method of sampling an analog signal, which overcomes the above mentioned problems.

In order to achieve said object the invention pro-vides a charge sampling (CS) circuit, comprising a control signal generator for controlling an analog input signal to the charge sampling circuit to be integrated by an inter-grator during a sampling phase responsive to a sampling

signal from the control signal generator, wherein the current of the analog input signal is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output at the end of the

5 sampling phase.

A more specific object of the invention is to provide a method and sampling circuit for band-pass sampling.

This object is achieved by a band-pass sampling (BPCS) circuit, comprising a control signal generator for

10 controlling a first and second end of a differential analog signal to be weighted by a weighting-and-sampling (W&S) element during a W&S phase responsive to a W&S signal from the control signal generator, wherein the current of the analog signal passes through said W&S element only when

15 said W&S signal is in a W&S phase, and said control signal generator is adapted for controlling the output signal of the W&S element to be integrated by an intergrator during the W&S phase, wherein the current of the output signal of the W&S element is integrated to an integrated charge for

20 producing a proportional voltage or current sample at a signal output at the end of the W&S phase.

Another more specific object of the invention is to provide a two-step BPCS circuit. This is achieved by a two-step BPCS circuit according to the invention, which

25 comprises a first BPCS circuit according to the invention for producing signal samples with a first sample rate; a chopping circuit for chopping the signal from the first BPCS circuit symmetrically in time at its signal output or output pair with the frequency of a clock signal equal to

30 the first sample rate; a differential-out amplifier for amplifying the signal from the chopping circuit differen-tially; wherein the first signal input and the second signal input of said second BPCS are connected to the signal output pair of said amplifier (41) for producing

signal samples at the signal output or output pair with a second sample rate.

A further specific object of the invention is to provide a front-end sampling radio receiver. This is
5 obtained by a front-end sampling radio receiver according to the invention, which comprises a low pass filter with a bandwidth up to twice the clock frequency for receiving and filtering a radio signal; a low noise amplifier for producing a differentially amplified radio signal from the
10 filtered signal; a local oscillator for producing an I-clock signal at its signal output; a $\pi/2$ phase shifter with a signal input connected to the local oscillator for producing a Q-clock signal at its signal output with the same amplitude and $\pi/2$ phase shift with respect to the
15 I-clock signal; wherein two ends of the signal output pair of said low noise amplifier are respectively connected both to the first BPCS circuit and the second BPCS circuit respectively, said I-clock signal output is connected to the clock input of said first BPCS circuit, and the Q-clock
20 signal output is connected to the clock input of the second BPCS circuit, for producing base-band I-samples of the radio signal at the signal output or output pair of the first BPCS circuit, base-band Q samples of the radio signal at the signal output or output pair of said second BPCS
25 circuit.

An advantage of the charge sampling circuit according to the invention is that the bandwidth of the charge sampling circuit does not have to be much larger than the signal bandwidth. Another important background is that for
30 a radio signal, no matter how high is the carrier frequency, the signal bandwidth (the base band) remains a small fraction of the full band between DC to the carrier frequency. It is therefore unnecessary to convert the full band but just the band with the signal.

The frequencies of the signals possibly to be sampled by the CS circuits or the BPCS circuits are higher or much higher than that of the voltage sampling circuits at a given accuracy.

The sampling capacitors used in the CS circuits or the BPCS circuits are larger or much larger than the ones used in the voltage sampling circuits, giving advantages of low noise and low clock-and-charge feed-through.

Each BPCS circuit is simultaneously a filter, a mixer and a sampler, which greatly simplifies a radio receiver.

The BPCS circuits are capable of directly working at the radio frequency band, which makes a highly digitized radio receiver with front-end sampling and A/D conversion possible.

Both the center frequency and the bandwidth of a BPCS circuit can be easily programmed. The bandwidth can be as narrow as required, equivalent to have an unlimited Q-value.

The CS and BPCS circuits are simple and can be easily implemented in CMOS or other processes.

This technique is very useful for the purpose of system-on-chip, which requires a simple and highly digitized architecture.

It should be emphasised that the term "comprises/ comprising" when used in this specification is taken to specify the presence of stated features, integers, steps or components and does not preclude the presence or addition of one or more other features, integers, steps, components or groups thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to explain the invention in more detail and the advantages and features of the invention a preferred embodiment will be described in detail below, reference be-ing made to the accompanying drawings, in which

FIG 1A is a block diagram of a first embodiment of a charge sampling (CS) circuit according to the invention,

FIG 1B shows the working waveforms of the charge sampling (CS) circuit in FIG 1A,

FIG 1C shows the frequency response of the charge sampling (CS) circuit in FIG 1A,

FIG 2A is a block diagram of a first embodiment of a a band pass charge sampling (BPCS) circuit according to the invention,

FIG 2B shows the working waveforms of the band pass charge sampling (BPCS) circuit in FIG 2A,

FIG 3 is a block diagram of a first embodiment of a differential BPCS circuit according to the invention,

FIG 4 is a block diagram of a first embodiment of a parallel differential BPCS circuit according to the invention

FIG 5 shows an illustration of the filter function for the BPCS circuits according to the invention

FIG 6A is the ideal frequency response of a constant-weighting BPCS circuit according to the invention with n=10,

FIG 6B is the output sample waveforms of a constant-weighting BPCS circuit with n=10,

FIG 7A is the ideal frequency responses of a constant-weighting BPCS circuit with n=50,

FIG 7B is the ideal frequency responses of a constant-weighting BPCS circuit with n=500,

FIG 8A is the ideal frequency responses of a linear-weighting BPCS circuit with n=50,

FIG 8B is the ideal frequency responses of a linear-weighting BPCS circuit with n=500,

FIG 9A is the ideal frequency responses of a Gauss-weighting BPCS circuit with n=75 and n=87,

FIG 9B is the ideal frequency responses of a Gauss-weighting BPCS circuit with n=750 and n=870,

FIG 10 is a circuit diagram of the first embodiment of the differential BPCS circuit in FIG 3,

FIG 11A shows the circuit diagram according to FIG 10 with n=10 in constant weighting at 1000 MHz

FIG 11B shows the resulting frequency response of the circuit in FIG 11A,

FIG 12A is the circuit diagram according to FIG 10 with n=59 in linear weighting at 1000 MHz,

FIG 12B is the resulting frequency response of the the circuit in FIG 12A,

FIG 13A is the circuit diagram according to FIG 10 with n=599 in linear weighting at 1000 MHz,

FIG 13B is the resulting frequency response of the circuit in FIG 13A,

FIG 14A is a circuit diagram of a single ended active integrator,

FIG 14B is a circuit diagram of a differential active integrator,

FIG 15 is a block diagram of a two-step BPCS circuit, and

FIG 16 is a block diagram of a front-end sampling radio receiver architecture.

DETAILED DESCRIPTION OF THE DRAWINGS

The present invention is a charge sampling (CS) circuit or a band-pass charge sampling (BPCS) circuit, sampling a signal by integrating its current in a given time window, and the resulting charge represents the signal sample at the center time of the window.

With reference to FIG 1A, a first embodiment of a charge sampling (CS) circuit 1 according to the invention is shown. It comprises sampling switch 2, an integrator 3 and a control signal generator 4. The switch 2 has a signal input, a signal output and a control input. An analog signal is applied to the signal input of the switch, which

is the signal input of the charge sampling circuit 1, and a
sampling signal is applied to the control input from the
control signal generator 4. The swith is on, i.e the signal
input is connected to the signal output of the switch, only

5   when the sampling signal is in the sampling phase. The
integrator 3 has a signal input, a signal output, and a
control input. The signal output of the switch 2 is applied
to the signal input of the integrator 3, and a resetting
signal from the control signal generator 4 is applied to

10   the control input of the integrator 3. The current of the
analog input signal to the CS circuit 1 is integrated
during sampling phase, and the integrated charge produces a
proportional voltage or current sample at the signal output
of the CS circuit at the end of the sampling phase. The

15   sample is held until the resetting phase of the resetting
signal begins, and the time interval in between is the
holding phase. A sequence of samples are produced when the
phases are repeated, and the signal output is the signal
output of said CS circuit. The control signal generator 4

20   has a clock input, which is the clock input of the CS
circuit, a sampling signal output connected to the control
input of the switch 2 and a resetting signal output
connected to the control input of the intergrator 3 as
mentioned above.

25   The the integrator 3 comprises a capacitor 3-1, a
resetting switch 3-2 and an optional resistor 3-3 in this
embodiment. The integrator 3 can, however, have a different
configuration in other embodiments. An analog signal is
applied to the input of the sampling switch 2. As

30   described, the charge sampling process involves three
successive phases: resetting, sampling (t_1 to t_2) and hold-
ing. The time from t_1 to t_2 is defined as the sampling
window. FIG. 1B shows its working waveforms. During the
resetting phase, only the resetting switch 3-2 is turned on

35   and the capacitor 3-1 is reset. During the sampling phase,

only the sampling switch 2 is turned on, and the signal
current is integrated onto the capacitor 3-1. The time
constant is large enough to be able to obtain a linear
charging when the signal comes from a voltage source (the
5   usual case). If the on-resistance of the switch 2 is too
small, the optional resistor 3-3 can be added. During the
holding phase, both switches are in off-state, and the
output voltage of the integrator 3 is held for further use.
A pair of interconnected CS circuits, forming a differen-
10   tial CS circuit, provide differential outputs to cancel
common mode effects, using a differential input signal and
sharing the control signal generator 4. The CS circuits or
circuit pairs are used in parallel to increase the sampling
rate and to make the time interval between two sampling
15   points possibly less than the sampling window, by
time-interleaving both sampling and resetting signals. The
signal current can be represented as $I(t)=\Sigma I_i \sin(\omega_i t+\phi_i)$,
i=1, 2, ..., m. The total integrated charge is $Q=\Sigma Q_i$ where
$Q_i=(I_i/\omega_i)(\cos(\omega_i t_1+\phi_i)-\cos(\omega_i t_2+\phi_i))$. If t_s is the center
20   time of the sampling window, and $2\Delta t=(t_2-t_1)$ is the window
width, $Q_1=(2\sin(\omega_i\Delta t/\omega_i)I_i\sin(\omega_i t_s+\phi_i)=2\Delta t(\sin(\omega_i\Delta t)/$
$(\omega_i\Delta t))I_i\sin(\omega_i t_s+\phi_i)$.

Compared with the instant value of the ith component
at t_s, $I_i(t_s)=I_i\sin(\omega_i t_s+\phi_i)$, the difference is
25   $k_i=2\Delta t(\sin(\omega_i\Delta t/\omega_i\Delta t))$, a sampling coefficient depending on
frequency ω_i and Δt. With this coefficient, the ith
frequency component has been precisely sampled at time t_s.
Since all frequency components are sampled at t_s, the total
charge on the capacitor naturally represents the signal
30   sample at t_s, i.e. t_s is the equivalent sampling time
point. The frequency response of the CS circuit depends on
the function $\sin(\omega_i\Delta t/\omega_i\Delta t)$, shown in FIG. 1C. Its 3 dB
bandwidth equals $\Delta f_{3dB}=1.4/(2\pi\Delta t)$, i.e. 1 GHz for a sampling
window of 450 ps, independent of resolution. For voltage
35   sampling, however, the sampling aperture must be smaller

than 1 ps for an 8-bit resolution at 1 GHz. Since the func-
tion $sin(\omega_i\Delta t/\omega_i\Delta t)$ is well defined, frequency compensation
becomes possible. One way is to let the analog signal pass
through a network with a frequency response of

5      $(\omega_i\Delta t)/sin(\omega_i\Delta t)$ before sampling. Another alternative is to
use digital signal processing (DSP) after A/D conversion to
compensate the frequency response.

Further, a band pass charge sampling (BPCS) circuit
comprises two switches, a weighting-and-sampling (W&S)

10   element, an integrator, and a control signal generator
generating a clock, an inverse clock, a W&S signal and a
resetting signal. Two ends of a differential signal are
applied to the two switch inputs respectively. The two
switches, controlled by the clock and the inverse clock

15   respectively, are turned on alternately. Both switch outputs
are fed to the W&S element input. The output of W&S element
is fed to the integrator input. It works in three
successive phases: resetting, sampling and holding. During
the resetting phase, the integrator is reset by the

20   resetting signal. Each sampling phase includes n clock
cycles, during which the signal current is weighted in the
W&S element and integrated in the integrator. During the
holding phase, the integrator output is held.

One embodiment of a band-pass charge sampling (BPCS)

25   circuit 5 is shown in FIG 2A. It comprises two switches 2A
and 2B, a weighting-and-sampling (W&S) element 6, an inte-
grator 3 and a control signal generator 7 generating a
clock, an inverse clock, a W&S signal and a resetting
signal. Two ends of a differential analog signal are

30   applied to the inputs of switches 2A and 2B respectively.
The switches 2A and 2B, controlled by the clock and the
inverse clock respectively, are turned on alternately. Both
outputs of switch 2A and 2B are fed to the input of W&S
element 6. The current passing through the W&S element 6 is

35   controlled by the W&S signal. The output of W&S element 6

is fed to the input of integrator 3. Three successive
phases are involved for each BPCS process: resetting,
sampling and holding. FIG. 2B shows the working waveforms.
During the resetting phase, the integrator is reset. Each
sampling phase includes n clock cycles forming a sampling
window. The signal current through W&S element equals zero
outside the sampling window and is weighted according to
the weighting function (constant, linear, Gauss or other
fuctions) within the sampling window. The weighting
function depends on the combination of the W&S element 6
and the W&S signal. The three W&S signals shown in FIG. 2B,
corresponding to the three weighting functions (constant,
linear and Gauss) are specifically used for a W&S element
in which the current is linearly controlled by the W&S
signal. During the holding phase, the output voltage of
integrator 3 is held for further use.

A differential BPCS circuit 8 is shown in FIG 3. It
comprises four switches 2A, 2B, 2C and 2D, a differential
W&S (D-W&S) element 9, a differential integrator 10, and a
control signal generator 7, as connected. The shown type of
D-W&S element 9 comprises two parallel W&S elements 6A and
6B, and the shown type of differential integrator comprises
two parallel integrators 3A and 3B. The D-W&S element 9 and
the differential integrator 10 may be in other types. The
differential BPCS circuit 8 works in the same way as the
single ended BPCS circuit 5 except to produce two outputs
differentially. The differential BPCS circuit 8 effectively
cancels the common mode effects and gives more accurate
results.

FIG 4 shows a parallel differential BPCS circuit 11.
It comprises four switches 2A, 2B, 2C and 2D, a number of
D-W&S elements 9A, 9B, ...,´ 9X, a number of differential
integrators 10A, 10B, ..., 10X, a multiplexer (MUX) 12 and
a control signal generator 13, as connected. Each pair of·
the D-W &S element and the differential integrator, 9A+10A,

9B+10B, ..., 9X+10X, together with the switches 2A, 2B, 2C
and 2D work in the same way as the differential BPCS
circuit 8. The W&S signals and the resetting signals to
these pairs, generated by the control signal generator 13,

5 are evenly time-interleaved. The MUX 12 multiplexes the
outputs of the differential integrators 10A, 10B, ..., 10X
to the differential outputs when they are in the holding
phase, controlled by the multiplexing signals from the
control signal generator 13. As a whole, the parallel BPCS

10 circuit gives a higher sampling rate and makes the time
interval between two successive sampling points possibly
less than the sampling window. If switches 2C and 2D are
removed, and the differential W&S elements and the differ-
ential integrators are replaced by single-ended versions,

15 it becomes a parallel single-ended BPCS circuit.

A filter function of the BPCS circuits is illustrated
in FIG 5. From top-down, the frequency increases from DC to
$3f_{,c}$ where f_c is the clock frequency. Note that during the
negative clock phase the same signal is connected oppo-

20 sitely, which is reflected in the diagram by changing the
signal sign. The normalized amplitudes of resulting
charges, i.e. the sums of the areas, integrated in n clock
cycles are listed in FIG 5 respectively. It is obvious that
for input signals with frequencies much higher or lower

25 than f_c, the charges cancel each other almost completely,
resulting in nearly zero output. For input signals with
certain frequencies like $f_c/4$, $f_c/2$, $2f_c$, ..., the charges
are completely cancelled no matter what are their phases.
For input signals with frequencies near to f_c, the charges

30 are only partly cancelled. When $f_{in}=f_c$, the charges are
fully added to each other if it is in-phase with f_c while
fully cancelled when it is in $\pi/2$ phase with f_c (not shown
in FIG. 5). There is a bandwidth in which the signal
charges can be effectively integrated. Outside the band-

35 width, the signal charges are either completely or substan-

tially cancelled. This is obviously a filter function. It means that the noise with frequencies outside the bandwidth will be cancelled as well.

An ideal frequency response of a BPCS circuit is shown in FIG 6A, which corresponds to a mathematically accurate integration of the signal current in the sampling window. In FIG 6A, n=10 and constant-weighting are assumed, meaning that the weight of the current is kept constant in the 10-clock-cycle sampling window. Further, FIG 6A shows the frequency response from $f_{in}=0$ to $f_{in}=8f_c$, where the y-axis is the maximum output amplitude of different frequency components normalized by the maximum output amplitude in the whole frequency range while the x-axis is input frequencies normalized by f_c. It can be seen that the same frequency response is repeated after $f_{in}>2f_c$ but with lower amplitudes. The output frequency f_{out} equals $|f_{in}-(2p-1)f_c|$ for $2(p-1)f_c \leq f_{in} \leq 2pf_c$, where p is an integer (≥ 1). When $f_{in}=(2p-1)f_c$, the output is a DC voltage, and its amplitude depends on the phase relation of f_{in} and f_c. For a given p, the same output frequency is obtained for input frequencies f_{in1} ($<(2p-1)f_c$) and f_{in2} ($>(2p-1)f_c$) when $(2p-1)f_c-f_{in1}=f_{in2}-(2p-1)f_c$, but their phases are different. FIG. 6B shows the output sample waveforms at different input frequencies with $f_c=1000$ MHz and both I (solid line) and Q (dots) phases. It shows that the BPCS circuit is a filter, a mixer and a sampler simultaneously.

In FIG 7A and FIG 7B, the ideal frequency responses of a constant-weighting BPCS circuit with n=50 and n=500 are shown respectively. FIG 7A shows the frequency response with n=50 in the range of $0< f_{in} <2f_c$ and in the fine range of $0.95f_c<f_{in}<1.05f_c$. FIG 7B shows the frequency response with n=500 in the range of $0<f_{in}<2f_c$ and in the fine range of $0.995f_c<f_{in}<1.005f_c$. It can be seen that $\Delta f_{3dB}=0.018f_c$ with n=50 and $\Delta f_{3dB}=0.0018f_c$ with n=500, i.e. the bandwidth is inversely proportional to n. The amplitudes of far-end

frequency components are reduced with the increase of n,
but the maximum adjacent peaks in both cases remain almost
unchanged, around -13 dB.

An ideal frequency responses of a linear-weighting
BPCS circuit with n=50 and n=500 are shown in FIG 8A and
FIG 8B, respectively. Linear-weighting means that during
the sampling phase the weight of the current is first
linearly increase and then linearly decrease, symmetric to
the center of the sampling window. FIG 8A shows the fre-
quency response with n=50 in the range of $0<f_{in}<2f_c$ and in
the fine range of $0.9f_c<f_{in}<1.1f_c$. FIG 8B shows the fre-
quency response with n=500 in the range of $0<f_{in}<2f_c$ and in
the fine range of $0.99f_c<f_{in}<1.01f_c$. It can be seen that
$\Delta f_{3dB}=0.025f_c$ with n=50 and $\Delta f_{3dB}=0.0025f_c$ with n=500,
slightly increasing compared to the constant-weighting
cases. The amplitudes of far-end frequency components are
rapidly reduced with the increase of n. The maximum adja-
cent peaks are reduced to -26 dB and -27 dB respectively,
compared to those of the constant-weighting cases.

In FIG 9A and FIG 9B, the ideal frequency responses
of a Gauss-weighting BPCS circuit are shown.
Gauss-weighting means that during the sampling phase the
weight of the current varies according to the Gauss func-
tion $\exp(-t^2/2\sigma^2)$ for a given σ, symmetric to the center of
the sampling window. The ratio $\Delta t/\sigma$, where Δt is half of
the sampling window and σ the standard deviation, is a
weighting parameter. FIG. 9A shows the frequency responses
of n=75 with $\Delta t/\sigma=3.5$ and n=87 with $\Delta t/\sigma=4$ respectively in
the range of $0<f_{in}<2f_c$. The 3 dB bandwidths are both
$0.025f_c$. FIG 9B shows the frequency responses of n=750 with
$\Delta t/\sigma=3.5$ and n=870 with $\Delta t/\sigma=4$ respectively in the range
of $0.9f_c<f_{in}<1.1 f_c$ The 3 dB bandwidths are both $0.0025f_c$.
The amplitudes of far-end frequency components and the
adjacent peaks are substantially reduced with the

Gauss-weighting. The maximum adjacent peaks are in the range of -61 dB to -78 dB.

An implementation 14 of the core of the differential BPCS circuit 8, using n-MOS transistors, is shown in FIG 10. The clocked switches are n-MOS transistors 15A, 15B, 15C and 15D. The W&S elements are n-MOS transistors 16A and 16B. The resetting switches are n-MOS transistors 18A and 18B. The capacitors are on-chip MOS capacitors 17A and 17B. The clocks are in sinuous waves but quasi-square waves can also be used. The implementation 14 works in all CMOS processes. Parameters of a 0.8 μm CMOS process, however, is used in the HSPICE simulations. The following three implementations are based on the implementation 14 with particular component values and W&S signal parameters.

An implementation 19 with n=10 in constant-weighting at f_c=1000 MHz is shown in FIG 11A,. The clocked switches are n-MOS transistors 20A, 20B, 20C and 20D. The W&S elements are n-MOS transistors 21A and 21B. The resetting switches are n-MOS transistors 23A and 23B. They all have the minimum size, 2 μm/0.8 μm (width/length). The capacitors are MOS capacitors 22A and 22B, both 40 pF. The width of the constant-weighting W&S signal is 10 ns, corresponding to n=10. The maximum differential output sample voltage is around 100 mV. FIG 11B shows both the theoretical frequency response in solid line and the HSPICE simulated frequency response in dots for f_{in}=900-1100 MHz. The simulated frequency response is closely in accordance with the theoretical frequency response. In both cases, the maximum adjacent peaks are -13 dB and Δf_{3dB}=18 MHz.

In FIG 12A, an implementation 24 with n=59 in linear-weighting at f_c=1000 MHz is shown. The clocked switches are n-MOS transistors 25A, 25B, 25C and 25D, all having an increased size of 10 μm/0.8 μm. This makes the signal currents dominated by the W&S elements not the switches. The W&S elements are n-MOS transistors 21A and

21B, 2 µm/0.8 µm. The resetting switches are n-MOS tran-
sistors 23A and 23B, 2 µm/0.8 µm. The capacitors are MOS
capacitors 22A and 22B, both 40 pF. The width of the
linear-weighting W&S signal is 59 ns, corresponding to

5   n=59. The maximum differential output sample voltage is
around 100 mV. FIG 12B shows the theoretical frequency
response in solid line and the HSPICE simulated frequency
response in dots for f_{in}=900-1100 MHz. The simulated
frequency response is basically in accordance with the

10   theoretical frequency response. Both have Δf_{3dB}=21 MHz. For
the implementation 24, however, the maximum adjacent peak
is -30 dB, lower than that of the theoretical response.
This is because the conductance of n-MOS transistors 21A or
21B does not vary linearly with the linear W&S signal. The

15   actual weighting function is somewhere between linear and
Gauss.

        An implementation 26 with n=599 in linear weighting
at f_c=1000 MHz is shown in FIG 13A. The clocked switches
are n-MOS transistors 25A, 25B, 25C and 25D, 10 µm/0.8 µm.

20   The W&S elements are n-MOS transistors 27A and 27B, 2 µm/16
µm. Note that the lengths of 27A and 27B are increased to
16 µm to limit the signal current and the capacitor voltage
dung such a long charging period (599 ns). The resetting
switches are n-MOS transistors 23A and 23B, 2 µm/0.8 µm.

25   The capacitors are MOS capacitors 28A and 28B, both 20 pF.
The width of the linear weighting W&S signal is 599 ns,
corresponding to n=599. The maximum differential output
sample voltage is around 100 mV. FIG 13B shows the
theoretical frequency response in solid line and the HSPICE

30   simulated frequency response in dots for f_{in}=990-1010 MHz.
The simulated frequency response is basically in accordance
with the theoretical frequency response. Both have Δf_{3dB}=2
MHz. For the same reason mentioned above, the maximum adja-
cent peak of the implementation 26 is -30 dB, lower than

35   that of the theoretical response.

FIG 14A and FIG 14B show active integrators for improving output swing and linearity, respectively. A single ended active integrator 29 is shown in FIG 14A. It comprises a differential-in-single-out amplifier 30, an
5 inverter 35, a capacitor 31, and switches 32, 33 and 34, as connected. An active integrator always keeps the signal input at virtual ground, eliminating the impact of capacitor voltage on the signal current. The bandwidth of amplifier 30 needs only to cover the signal base-band not the
10 carrier, which makes it feasible. The inverter 35 produces an inverted resetting signal with a delay, using the resetting signal as the input, to control the switch 33 while the resetting signal controls the switches 32 and 34. During the resetting phase, the switches 32 and 34 are
15 turned on, and the switch 33 is turned off. The voltage of capacitor 31 is reset to the input offset voltage of the amplifier 30. During the sampling phase, the switches 32 and 34 are turned off and the switch 33 is turned on. The capacitor 31 is charged by the signal current. In the same
20 time, the offset voltage of the amplifier 30 is cancelled. A differential active integrator 36 is shown in FIG 14B. It comprises a differential-in-differential-out amplifier 37, two capacitors 31A and 31B, an inverter 35, and switches 32A, 32B, 33A, 33B, 34A and 34B. It works basically in the
25 same way as the integrator 29 except uses a differential input signal and gives differential outputs. The integrator 29 can replace the integrator 3 in FIG 1A while the integrator 36 can replace the integrator 10 in FIG 3.

FIG 15 shows a two-step BPCS circuit 38. It comprises
30 a first BPCS circuit 39, a chopping circuit 40, an amplifier 41, a second BPCS circuit 42, and a clock signal generator 43 generating a second clock. The first BPCS circuit 39 and the second BPCS circuit 42 can be any type of the BPCS circuits 5, 8, 11, 19, 24 and 26. To the first
35 BPCS circuit 39, two ends of a differential analog signal

are applied to its two inputs respectively, and a first
clock is applied to its clock input. Signal samples with a
first sample rate are produced from the first BPCS circuit
39 and fed to the chopping circuit 40. The samples are
5   chopped symmetrically in time, controlled by the second
clock. From the chopping circuit 40, the chopped signal
with a new carrier frequency equal to the chopping fre-
quency is fed to the amplifier 41, and the amplified
differential signals are fed to two inputs of second BPCS
10   circuit 42 respectively. Controlled by the second clock,
the second BPCS circuit 42 produces the final sample output
with a second sample rate. The two-step BPCS circuit 38
gives flexibility in performance trade-off. BPCS circuits
in more steps can be built based on the two-step BPCS
15   circuit 38.

A front-end sampling radio receiver architecture 44
is shown in FIG 16. It comprises a low pass filter 45 with
$f_{pass}<2f_c$ a differential-out low noise amplifier (LNA) 46,
two BPCS circuits 47A and 47B, a 90° phase shifter 48, and
20   a local oscillator 49. The radio signal from antenna is
applied to the input of the low pass filter 45. The fre-
quency components above $2f_c$ are greatly attenuated. The
output of the low pass filter 45 is fed to the LNA 46 to
produce differential outputs with a large enough amplitude.
25   The differential outputs are fed to the inputs of BPCS
circuits 47A and 47B simultaneously. In the same time, the
I-clock signal produced by the local oscillator 49 is fed
to the BPCS circuit 47A while the Q-clock signal reproduced
by the 90° phase shifter 48 from the I-clock signal is fed
30   to the BPCS circuit 47B. The BPCS circuits 47A and 47B
produce I-samples and Q-samples respectively. The sample
outputs can be either converted to digital data immediately
or further treated. The BPCS circuits 47A and 47B can be
any of the BPCS circuits 5, 8, 11, 19, 24 and 26. The inte-
35   grators in these circuits can be either passive integrators

or active integrators. The radio receiver architecture 44 has filtering, mixing and sampling functions simultaneously at the front-end, which relaxes the performance demands on A/D conversion, avoids analog filters, and highly utilizes the capability of DSP. In principle, any narrow bandwidth, i.e. any high Q value, is possible. The center frequency of the filtering function can be easily programmed. It is indeed a superior radio receiver architecture with a wide application scope.

The sampling capacitors used in the CS and the BPCS circuits are much larger than that used in a voltage sampling circuit, resulting in low noise and low charge and clock feed-through.

The BPCS circuit is simultaneously a filter, a mixer and a sampler, capable of working at radio frequencies. The center frequency, the bandwidth and the adjacent selectivity can be set by the clock frequency, the number n and the shape of W&S signal, particularly useful for front-end sampling radio receiver and system-on-chip.

It is to be understood that even though numerous characteristics and features of the present invention have been set forth in the description, together with details of the function of the invention, the disclosure is illustrative only and changes may be made in detail within the scope of the invention defined by the following claims.

CLAIMS

1. A charge sampling (CS) circuit (1), **characterised** by a control signal generator (4) for controlling an analog input signal to the charge sampling circuit (1) to be inte-

5 grated by an intergrator (3) during a sampling phase responsive to a sampling signal from the control signal generator (4), wherein the current of the analog input signal is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output

10 at the end of the sampling phase.

2. A charge sampling (CS) circuit (1) according to claim 1, **characterised** by a sampling switch (2) having a signal input for analog input signals, a signal output

15 connected to a signal input of said integrator (3), and a control input connected to a sampling signal output of said control signal generator (4) for controlling the switch to be on only when said sampling signal from the generator (4) is in a sampling phase.

20

3. A charge sampling (CS) circuit (1) according to claim 1 or 2, **characterised** in that the control signal generator (4) is adapted to control the integrator (3) to hold the sample until a resetting signal from the generator

25 (4) is applied to a control input of the integrator (3).

4. A charge sampling (CS) circuit (1) according to any of the claims 1-3, **characterised** in that
if said sampling phase is from time t_1 to time t_2,

30 said sample represents the instant value of said analog signal at time $t_s = (t_1, + t_2)/2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin(2\pi f_i \Delta t))/(2\pi f_i \Delta t)$, where f_i is the frequency of the ith component of said analog signal

and $\Delta t = (t_2 - t_1)/2$, i.e half of the width of said sampling phase.

5. A differential charge sampling (CS) circuit, **char-acterised** by a first and second CS circuit according to any of the claims 1-4 having, wherein all control signal generators of said CS circuits are replaced by a common control signal generator (4), the signal input of said first CS circuit is a first analog input of said differential CS circuit, the signal input of said second CS circuit is a second input of said differential CS circuit for a differential analog signal, the signal output of said first CS circuit and the signal output of said second CS circuit are the first signal output and the second signal output of said differential CS circuit.

6. A differential charge sampling (CS) circuit according to claim 5, **characterised** in that the integrator (3) of said first CS circuit and the integrator (3) of said second CS circuit forming a single differential integrator with two inputs for integrating the differential current of said analog signal and producing differential samples at said first signal output and a second signal output.

7. A band-pass charge sampling (BPCS) circuit (5), **characterised** by a control signal generator (7) for controlling a first and second end of a differential analog signal to be weighted by a weighting-and-sampling (W&S) element (6) during a W&S phase responsive to a W&S signal from said control signal generator (7), wherein the current of said analog signal passes through said W&S element (6) only when said W&S signal is in a W&S phase, and said control signal generator (7) is adapted for controlling the output signal of said W&S element (6) to be integrated by an intergrator (3) during said W&S phase, wherein the

current of the output signal of said W&S element (6) is integrated to an integrated charge for producing a proportional voltage or current sample at a signal output at the end of said W&S phase.

8. A band-pass charge sampling (BPCS) circuit (5) according to claim 7, **characterised** by a first switch (2A) having a signal input for receiving a first end of said differential analog signal, a signal output connected to a signal input of said Weighting-and- sampling (W&S) element (6), and a control input connected to a clock output of said control signal generator (7) for controlling the switch (2A) to be on only when a clock signal is received, a second switch (2B) having a signal input for receiving a second end of said differential analog signal, a signal output connected to said signal input of said Weighting-and-sampling (W&S) element (6), and a control input, connected to an inverse clock output output of said control signal generator (7) for controlling the switch (2B) to be on only when a clock signal is received, said weighting-and-sampling (W&S) element (7) having a control input connected to a W&S signal output of said control signal generator, wherein the current of said analog signal passes through said W&S element (6) only when said W&S signal is in a W&S phase containing n cycles of said clocks, and the current of said analog signal is controlled by said W&S signal in constant, linear, Gauss or other weighting functions, and an integrator with a signal input connected to the output of said W&S element (6), a control input connected to a resetting signal output of said control signal generator (7).

9. A band-pass charge sampling (BPCS) circuit (5) according to claim 7 or 8, **characterised** in that the control signal generator (7) is adapted to control the inte-

grator to hold the sample until the resetting phase of said
resetting signal begins.

      10. A band-pass charge sampling (BPCS) circuit (5)
according to any of the claims 7-9, **characterised** in that
said samples represent the base-band content of said analog
signal, and the output frequency is $f_{out}=|f_{in}-(2p-1)f_c|$ for $2(p-1)f_c \leq f_{in} \leq pf_c$, where f_{in} is one of the frequency components of
said analog signal, f_c the frequency of said clock and p an
integer of ≥ 1 respectively, and the phase of said output
frequency depends on the phase of said f_{in} and the phase of
said f_c and p=1 defines the major frequency response range,
and the same shape of frequency response is repeated for
p>1 but the amplitudes arc reduced, and for a given p, the
same output frequency is obtained for frequencies f_{in1}
$(<(2p-1)f_c)$ and f_{in2} $(>(2p-1)f_c)$ when $(2p-1)f_c-f_{in1}=f_{in2}-(2p-1)f_c$ but with different phases, and the bandwidth
and the shape of said frequency response depend on said n
(the lager n, the narrower bandwidth) and said weighting
function (constant, linear, Gauss or other functions), and
said BPCS circuit is simultaneously a filter, a mixer and a
sampler.

      11. A differential band-pass charge sampling (BPCS)
circuit (8), **characterised** by a first and second BPCS cir-
cuit according to any of the claims 7-10, wherein all con-
trol signal generators of said BPCS circuits are replaced
by a common control signal generator (7), the first signal
input and the second signal input of said first BPCS cir-
cuit are connected with the second input and the first
input of said first BPCS circuit respectively, and the
first signal input, the second signal input, the signal
output of said first BPCS circuit and the signal output of
said second BPCS circuit are the first signal input, the
second signal input, the first signal output and the second

signal output of said differential band-pass charge
sampling (BPCS) circuit.

12. A differential band-pass charge sampling (BPCS)
circuit (8) according to claim 11, **characterised** in that
the integrators (3A,3B) in said first BPCS circuit and said
second BPCS circuit are merged into a single differential
integrator (10) integrating the differential current of
said analog signal and producing differential samples at
said first signal output and said second signal output of
said differential BPCS circuit.

13. A parallel CS circuit, comprising a number of CS
circuits according to any of the preceding claims 1-4,
characterised in that all first signal inputs are
connected together as a first analog signal input of said
parallel CS circuit, all control signal generators of said
CS circuits are replaced by a common control signal gener-
ator, a multiplexer having said number signal inputs
connected to the signal outputs of said CS circuits respec-
tively, control inputs connected to multiplexing signal
outputs of said common control signal generator, and a
signal output, for multiplexing the outputs of said CS
circuits to the output of said parallel CS circuit when the
outputs of said CS circuits are in holding phases, wherein
said parallel CS circuit increases the sampling rate and
makes the time interval between two successive sampling
points short, and the parallel CS circuit is in a single
ended version.

14. A parallel CS circuit, comprising a number of
differential CS circuits according to claim 5 or 6, **charac-
terised** in that all first inputs are connected together as
the first signal input of said parallel CS circuit for
receiving a first end of a differential analog signal, all

second inputs are connected together as the second signal input of said parallel CS circuit for receiving a second end of said differential analog signal, and all control signal generators of said CS circuits are replaced by a

5 common control signal generator, a multiplexer having said number signal input pairs connected to the signal output pairs of said CS circuits respectively, control inputs connected to multiplexing signal outputs of said common control signal generator, and a signal output pair, for

10 multiplexing the output pairs of said CS circuits to the output pair of said parallel CS circuit when the output pairs of said CS circuits are in holding phases, wherein said parallel CS circuit increases the sampling rate and makes the time interval between two successive sampling

15 points short, and the parallel CS circuit is in a differential version.

15. A parallel CS circuit according to claim 13 or 14, **characterised** in that said control signal generator

20 has a clock input, said number of sampling signal outputs, said number of resetting signal outputs and said number of multiplexing signal outputs, for generating said number of sampling signals at the sampling signal outputs connected to the control inputs of the switches of said CS circuits

25 respectively, and for generating said number of resetting signals at said resetting signal outputs connected to the control inputs of the integrators of the CS circuits respectively, and said number of multiplexing signals are generated at the multiplexing signal outputs, and said

30 resetting signals, said sampling signals and said multiplexing signals are evenly timeinterleaved.

16. A parallel BPCS circuit (11) comprising a number of BPCS circuits according to claim 7-10, **characterised** in

35 that all first signal inputs are connected together as the

first signal input of said parallel BPCS circuit for
receiving a first end of a differential analog signal, all
second signal inputs are connected together as the second
signal input of said parallel BPCS circuit for receiving a
5 second end of a differential analog signal, and all the
first switches are separate or merged, and all the second
switches are separate or merged, and all control signal
generators in said BPCS circuits are replaced by a common
control signal generator (13), and a multiplexer (11)
10 having said number of signal inputs connected to the signal
outputs of said BPCS circuits, control inputs connected to
multiplexing signal outputs of said common control signal
generator, and a signal output, for multiplexing the
outputs of said BPCS circuits to the signal output when the
15 signal outputs of said BPCS circuits are in holding phases,
wherein the signal output is the signal output of said
parallel BPCS circuit, and said parallel BPCS circuit
increases the sampling rate and makes the time interval
between two successive sampling points smaller, and the
20 parallel BPCS circuit is in a single ended version.

17. A parallel BPCS circuit (11) comprising a number
of BPCS circuits according to claim 11 or 12, **characterised**
in that all first signal inputs are connected together as
25 the first signal input of said parallel BPCS circuit for
receiving a first end of a differential analog signal, all
second signal inputs are connected together as the second
signal input of said parallel BPCS circuit for receiving a
second end of a differential analog signal, all the first
30 switches in said first BPCS circuits are separate or
merged, all the second switches in said first BPCS circuits
are separate or merged, all the first switches in said
second BPCS circuits are separate or merged, all the second
switches in said second BPCS circuits are separate or
35 merged, all control signal generators of said BPCS circuits

are replaced by a common control signal generator, and a multiplexer with said number of signal input pairs connected to the signal output pairs of said BPCS circuits, control inputs connected to multiplexing signal outputs of

5   said common control signal generator, and an output pair, for multiplexing the output pairs of said BPCS circuits to the signal output pair when the signal output pairs of said BPCS circuits are in holding phases, wherein the signal output pair is the signal output pair of said parallel BPCS

10   circuit, and said parallel BPCS circuit increases the sampling rate and makes the time interval between two successive sampling points smaller, wherein the parallel BPCS circuit is in a differential version.

15   18. A parallel BPCS circuit comprising a number of BPCS circuits according to claim 16 or 17, **characterised** by a control signal generator with a clock input, a clock output, an inverse clock output, said number of W&S signal outputs, said number of resetting signal outputs and said

20   number of multiplexing signal outputs, wherein the clock input is the clock input of said parallel BPCS circuit for use in generating a clock signal at the clock output of said common signal control generator connected to the control inputs of all first switches of said BPCS circuits,

25   and an inverse clock at the inverse clock output connected to the control inputs of all second switches of said BPCS circuits, said number of W&S signal outputs are connected to the control inputs of all W&S elements (9A-9X) of said BPCS circuits, said number of resetting signal outputs are

30   connected to the control inputs of all integrators (10A-10X) of said BPCS circuits, and said number of multiplexing signals, resetting signals, sampling signals, and multiplexing signals are evenly timeinterleaved.

19. A CS circuit according to any of the claims 1-4,
or 13, **characterised** by an analog frequency compensating
circuit having a signal input for receiving an analog
signal, and a signal output, with a frequency response pro-
portional to $(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$, wherein the signal
output is connected to the signal input of said CS.

20. A CS circuit according to any of the claims 5,
6, or 14, **characterised** by an analog frequency
compensating circuit having a signal input pair for
receiving an analog signal, and a signal output pair, with
a frequency response proportional to $(2\pi f_i \Delta t)/$
$(\sin(2\pi f_i \Delta t))$, wherein the signal output pair is connected
to the first signal input and the second signal input of
said CS circuit.

21. A CS circuit according to any of the claims 1-4,
or 13, **characterised** by a digital frequency compensating
circuit with a frequency response proportional to
$(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$ connected after an A/D converter
converting the signal output of said CS circuits to a
digital signal.

22. A CS circuit according to any of the claims 5-6,
or 14, **characterised** by a digital frequency compensating
circuit with a frequency response proportional to
$(2\pi f_i \Delta t)/(\sin(2\pi f_i \Delta t))$ connected after an A/D converter
converting the signal output pair of said CS circuits to a
digital signal.

23. A two-step BPCS circuit comprising a first and
second BPCS circuit (39,42) according to any of the preced-
ing claims 6-12 or 16-18, **characterised** by
a first signal input and a second signal input for
receiving a first and second end of a differential analog

signal, respectively, in said first BPCS circuit (39) for
producing signal samples at the signal output or output
pair of said first BPCS circuit with a first sample rate;

5   a chopping circuit (40) for chopping the signal from
the first BPCS circuit (39) symmetrically in time at its
signal output or output pair with the frequency of a clock
signal equal to said first sample rate,

          a differential-out amplifier (41) for amplifying the
signal from the chopping circuit differentially at its
10   signal output pair; and

          the first signal input and the second signal input of
said second BPCS are connected to the signal output pair of
said amplifier (41) for producing signal samples at the
signal output or output pair with a second sample rate.

15

          24. A two-step BPCS circuit comprising according to
claim 23, **characterised** by a clock signal generator (43)
having a clock input for receiving a first clock signal
used by the first BPCS circuit (39), and generating a
20   second clock signal simultaneously fed to a clock input of
said chopping circuit and a clock input of said second BPCS
circuit.

          25. Arrangements of building blocks in any type of
25   said BPCS circuits according to claims 1-24, **characterised**
by

          an n-MOS arrangement of said switch, comprising: an
n-MOS transistor with the drain as the signal input, with
the gate as the control input and with the source as the
30   signal output; and

          a CMOS arrangement of said switch, comprising: an
n-MOS transistor and a p-MOS transistor with their drains
connected to each other as the signal input, with their
sources connected to each other as the signal output, and
35   with the gate of said n-MOS transistor as the control

input; an inverter with the input connected to the gate of
said n-MOS transistor and with the output connected to the
gate of said p-MOS transistor;

     an arrangement of said W&S element, comprising: an
5   n-MOS transistor with the drain as the signal input, with
the gate as the control input, and with the source as the
signal output;

     a passive arrangement of said integrator, comprising:
a capacitor with the first end as the signal input, and
10   with the second end grounded; an optional resistor inserted
between said signal input and the first end of said
capacitor when necessary; an n-MOS transistor with the
drain and the source connected to the first end and second
end of said capacitor respectively, and with the gate as
15   the control input;

     a passive arrangement of said differential integrator
comprising: a first passive arrangement of said integrator
with the signal input and the signal output as the first
signal input and the first signal output of said
20   differential integrator respectively; and a second passive
arrangement of said integrator with the signal input and
the signal output as the second signal input and the second
signal output of said differential integrator respectively;

     an active arrangement of said integrator comprising:
25   a differential-in-single-out amplifier with the positive
input grounded, with the negative input as the signal input
of said integrator, and with the output as the signal
output of said integrator; a capacitor with the first end
connected to the negative input of said
30   differential-in-single-out amplifier; an inverter with the
input as the control input of said integrator; a first
n-MOS arrangement or CMOS arrangement of said switch with
the signal input connected to the negative input of said
differential-in-single-out amplifier, with the control
35   input connected to the control input of said integrator,

and with the signal output connected to the output of said
differential-in-single-out amplifier; a second n-MOS
arrangement or CMOS arrangement of said switch with the
signal input connected to the second end of said capacitor,
5   with the control input connected to the control input of
said integrator, and with the signal output grounded; a
third n-MOS arrangement or CMOS arrangement of said switch
with the signal input connected to the second end of said
capacitor, with the control input connected to the output
10   of said inverter and with the signal output connected to
the output of said differential-insingle-out amplifier; and
an optional resistor inserted between the signal input of
said integrator and the negative input of said
differential-in-single-out amplifier when necessary;
15   an active arrangement of said differential
integrator, comprising: a differential-in-differential-out
amplifier with the negative input, the positive input, the
positive output and the negative output as the first signal
input, the second signal input, the first signal output and
20   the second signal output of said differential integrator; a
first capacitor with the first end connected to the
negative input of said differential-indifferential-out
amplifier; a second capacitor with the first end connected
to the positive input of said differential-in-
25   differential-out amplifier; an inverter with the input as
the control input of said differential integrator; a first
n-MOS arrangement or CMOS arrangement of said switch with
the signal input connected to the negative input of said
differential-in-differential-out amplifier, with the
30   control input connected to the control input of said
differential integrator and with the signal output
connected to the positive output of said differen-
tial-in-differential-Out amplifier; a second n-MOS arrange-
ment or CMOS arrangement of said switch with the signal
35   input connected to the second end of said first capacitor,

with the control input connected to the control input of
said differential integrator and with the signal output
grounded; a third n-MOS arrangement or CMOS arrangement of
said switch with the signal input connected to the second
5   end of said first capacitor, with the control input
connected to the output of said inverter and with the
signal output connected to the positive output of said
differential-in-differential-out amplifier; a fourth n-MOS
arrangement or CMOS arrangement of said switch with the
10   signal input connected to the positive input of said
differential-in-differential-out amplifier, with the
control input connected to the control input of said
differential integrator and with the signal output
connected to the negative output of said differen-
15   tial-in-differential-out amplifier; a fifth n-MOS arrange-
ment or CMOS arrangement of said switch with the signal
input connected to the second end of said second capacitor,
with the control input connected to the control input of
said differential integrator and with the signal output
20   grounded; a sixth n-MOS arrangement or CMOS arrangement of
said switch with the signal input connected to the second
end of said second capacitor, with the control input
connected to the output of said inverter and with the
signal output connected to the negative output of said
25   differential-in-differential-out amplifier; a first
optional resistor inserted between the first signal input
of said differential integrator and the negative input of
said differential-in-differential-out amplifier when
necessary; and a second optional resistor inserted between
30   the second signal input of said differential integrator and
the positive input of said differential-in-differential-out
amplifier when necessary.

26. A front-end sampling radio receiver apparatus comprising a first and second BPCS circuit according to claims 7-12,16-18,23,24, **characterised** by comprising:

a low pass filter (45) with a bandwidth up to twice
5   the clock frequency for receiving and filtering a radio signal;

a low noise amplifier (46) for producing a differentially amplified radio signal from the filtered signal;

a local oscillator (49) for producing an I-clock
10   signal at its signal output;

a $\pi/2$ phase shifter (48) with a signal input connected to the local oscillator (49) for producing a Q-clock signal at its signal output with the same amplitude and $\pi/2$ phase shift with respect to said I-clock signal;

15   two ends of the signal output pair of said low noise amplifier (46) are respectively connected both to the first BPCS circuit (47A) and the second BPCS circuit (47B) respectively, said I-clock signal output is connected to the clock input of said first BPCS circuit (47A), and said
20   Q-clock signal output is connected to the clock input of said second BPCS circuit (47B), for producing base-band I-samples of said radio signal at the signal output or output pair of said first BPCS circuit (47A), base-band Q - samples of said radio signal at the signal output or output
25   pair of said second BPCS circuit (47B).

27. A front-end sampling radio receiver apparatus according to claim 26, **characterised** in that

said local oscillator (49), said phase shifter (48)
30   and the clock generators of said first and second BPCS circuits (47A,47B) are combined for producing differential I-clock signals and Q-clock signals more efficiently and accurately;

said base-band I-sample and Q-samples are converted
35   either by two separate analog-to-digital converters or by a

single analog-to-digital converter with multiplexing to digital signals;

said digital signals are processed by a digital signal processing (DSP) unit; and

said front-end sampling radio receiver apparatus is a superior radio receiver apparatus having a greatly simplified analog part and wherein the capability of DSP is highly utilized.

28. A method of charge sampling, **characterised** by the steps of:

integrating an analog input signal during a sampling phase, wherein the current of the analog input signal is integrated to an integrated charge, and

producing a proportional voltage or current sample of said integrated charge at the end of said sampling phase.

29. A method according to claims 28, **characterised** in that, if said sampling phase is from time t_1 to time t_2, said sample represents the instant value of said analog signal at time $t_s = (t_1, +t_2)/2$ and differs from said instant value with a coefficient consisting of a constant part and a frequency dependent part $(\sin(2\pi f_i\Delta t))/(2\pi f_i\Delta t)$, where f_i is the frequency of the ith component of said analog signal and $\Delta t = (t_2-t_1)/2$, i.e half of the width of said sampling phase.

30. A method according to claim 28 or 29, **characterised** in that said analog input signal is a differential analog signal, and said proportional voltage or current sample of said integrated charge is a differential signal.

31. A method of charge sampling, **characterised** by the steps of: weighting a first and second end of a differential analog signal during a W&S phase, integrating the

weighted signal during said W&S phase, wherein the current
of the weighted signal is integrated to an integrated
charge; and

     producing a proportional voltage or current sample at
5 the end of said W&S phase.

FIG. 1A
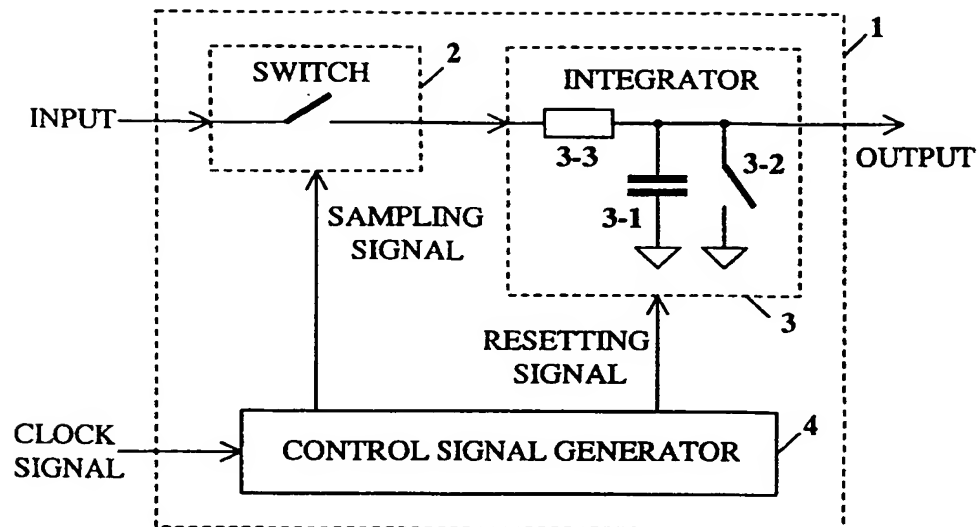
FIG. 1B
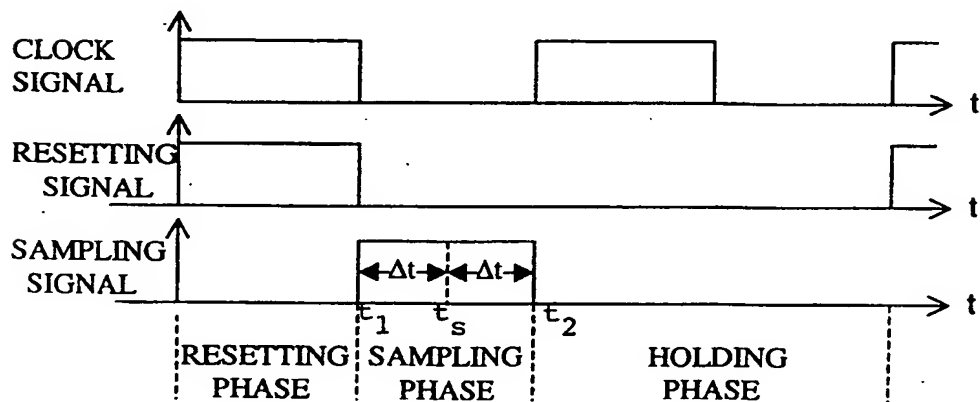
FIG. 1C
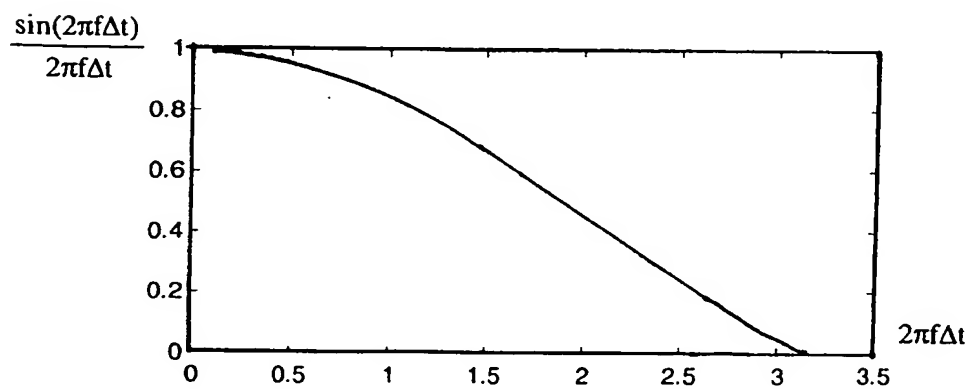
2/16
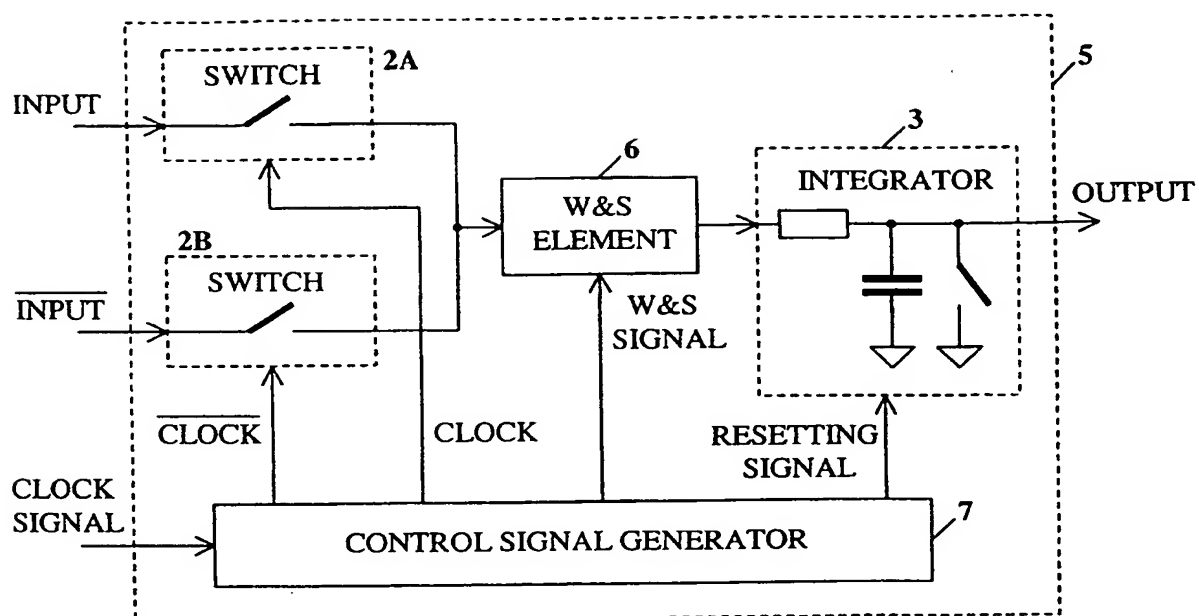
FIG. 2A
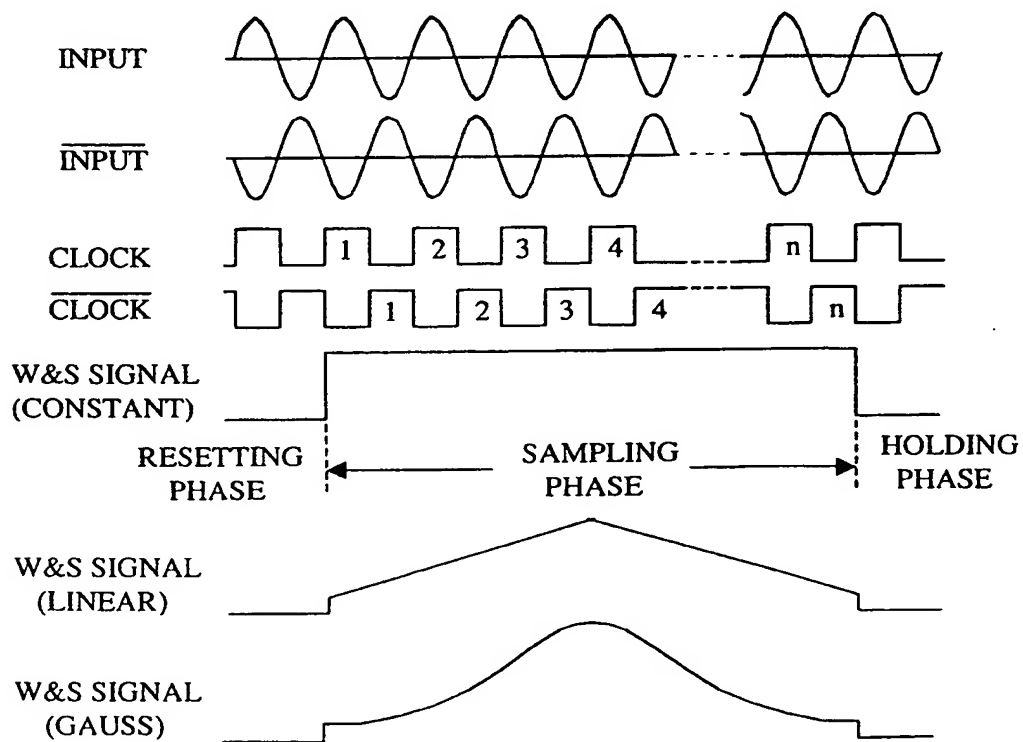
FIG. 2B
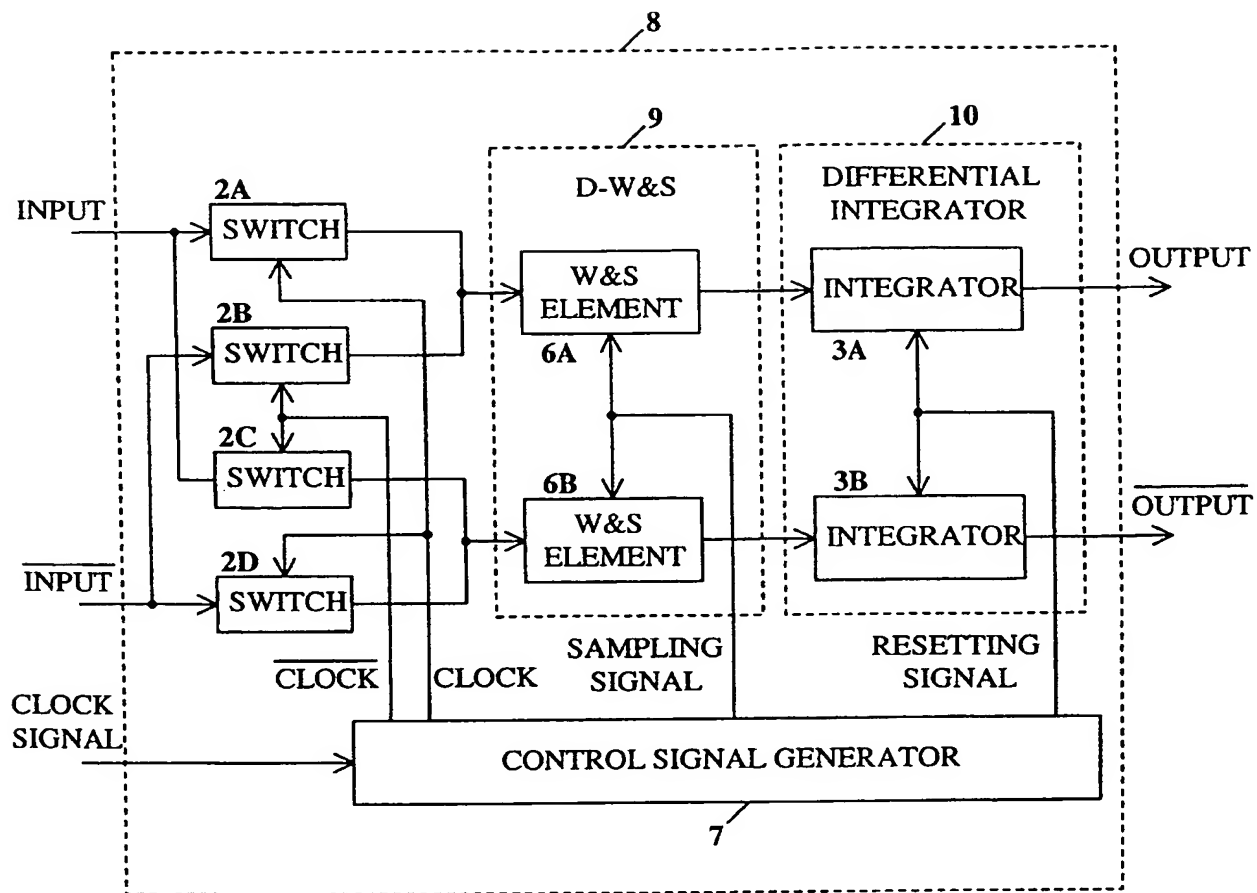
FIG. 3
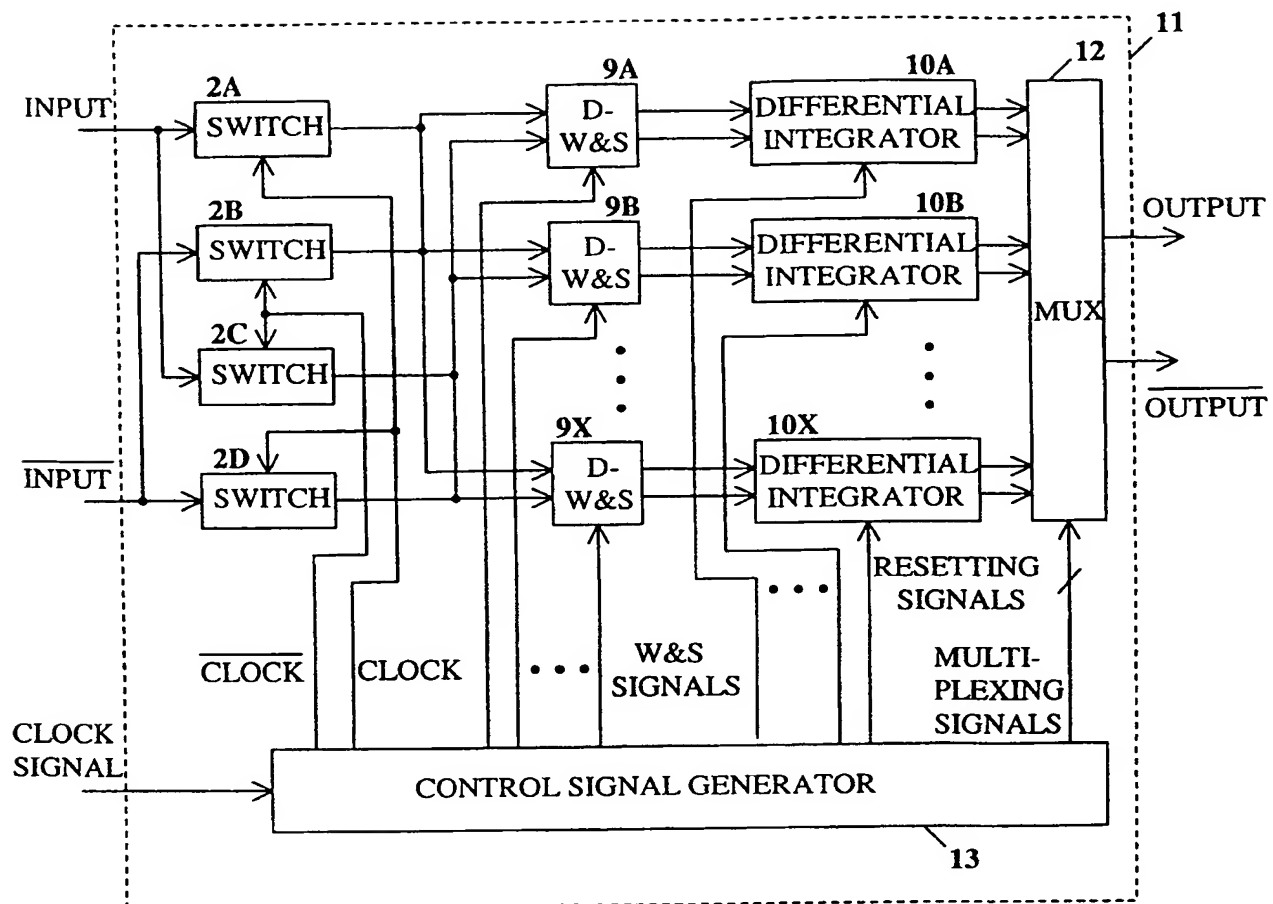
FIG. 4
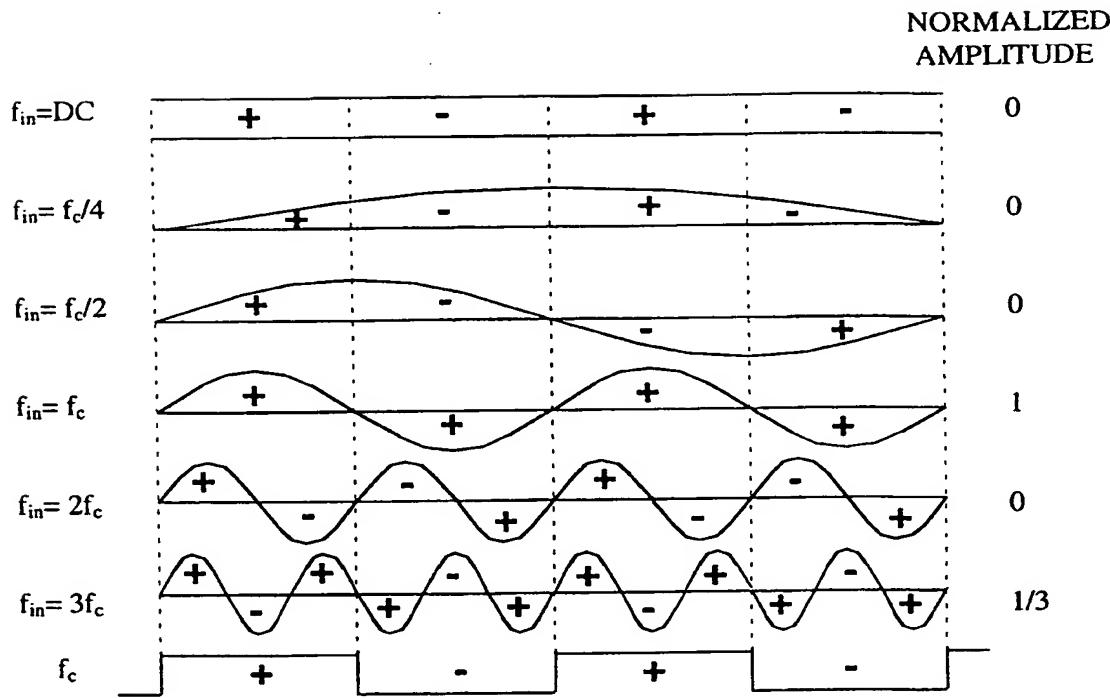
FIG. 5

NORMALIZED
AMPLITUDE

FIG. 6A

NORMALIZED FREQUENCY (f_{in}/f_c)
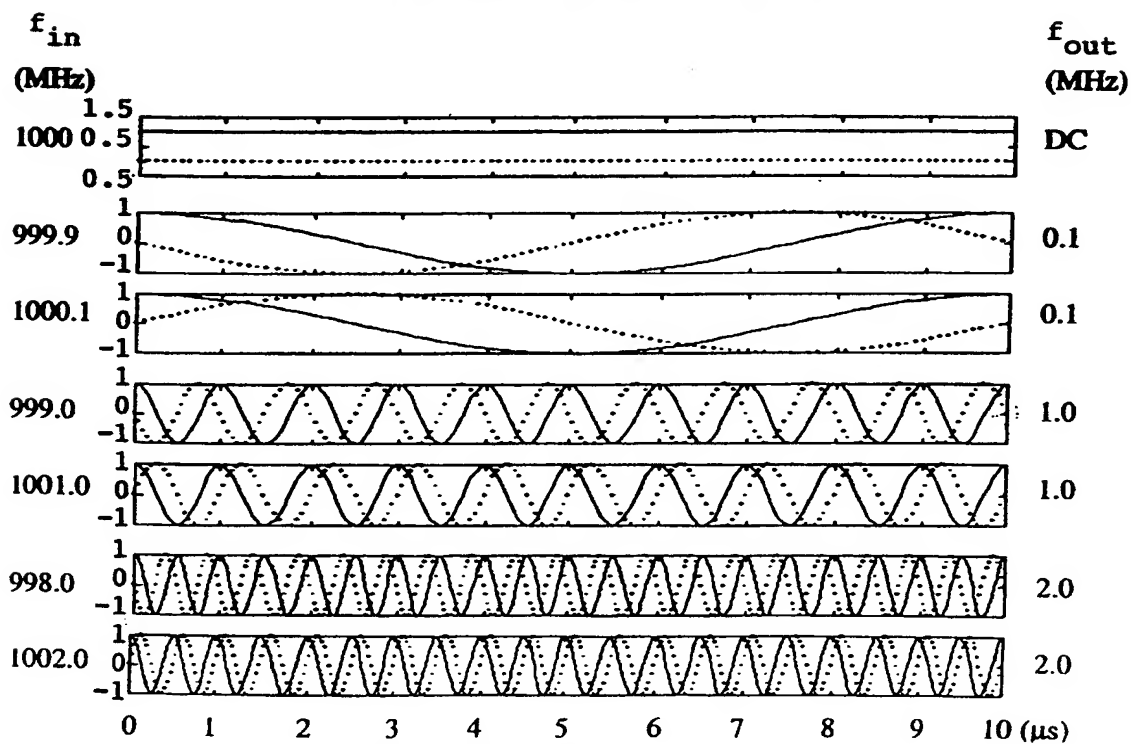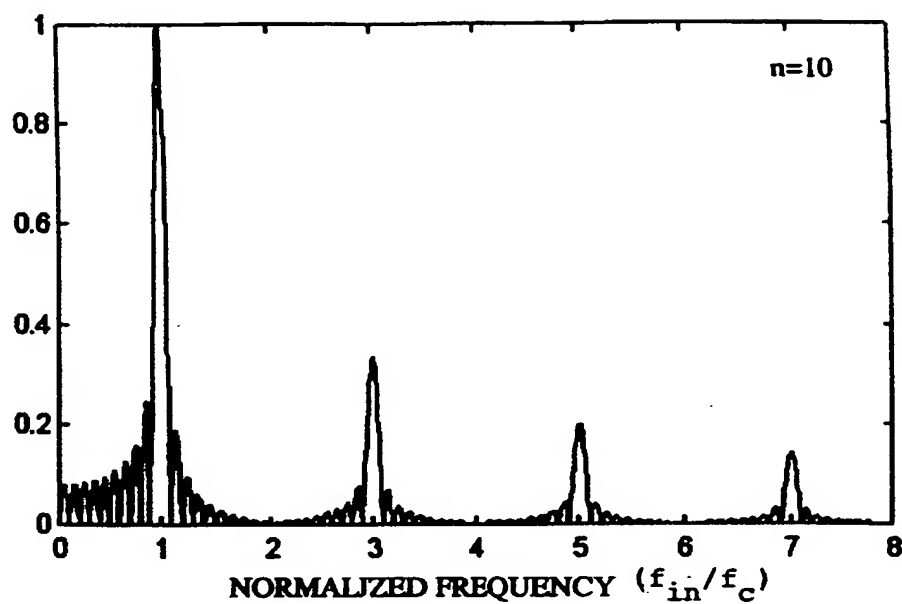
Note: 1. f_c=1000 MH$_z$.

2. I in solid line and Q in dash line.

FIG. 6B
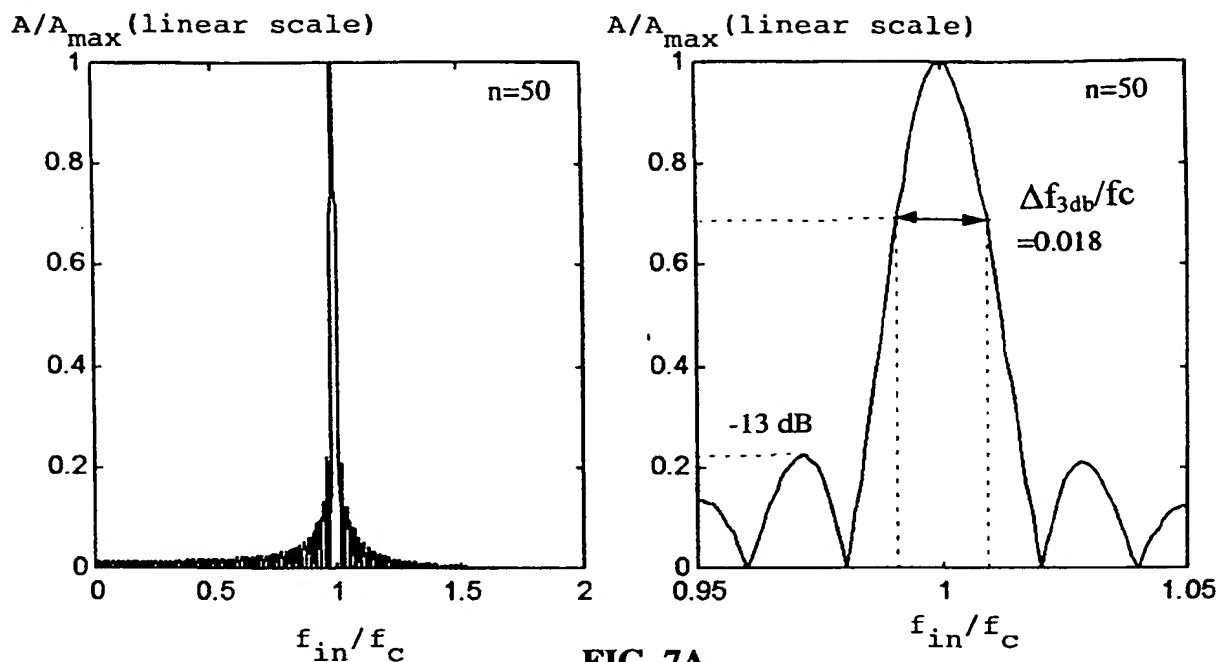
FIG. 7A
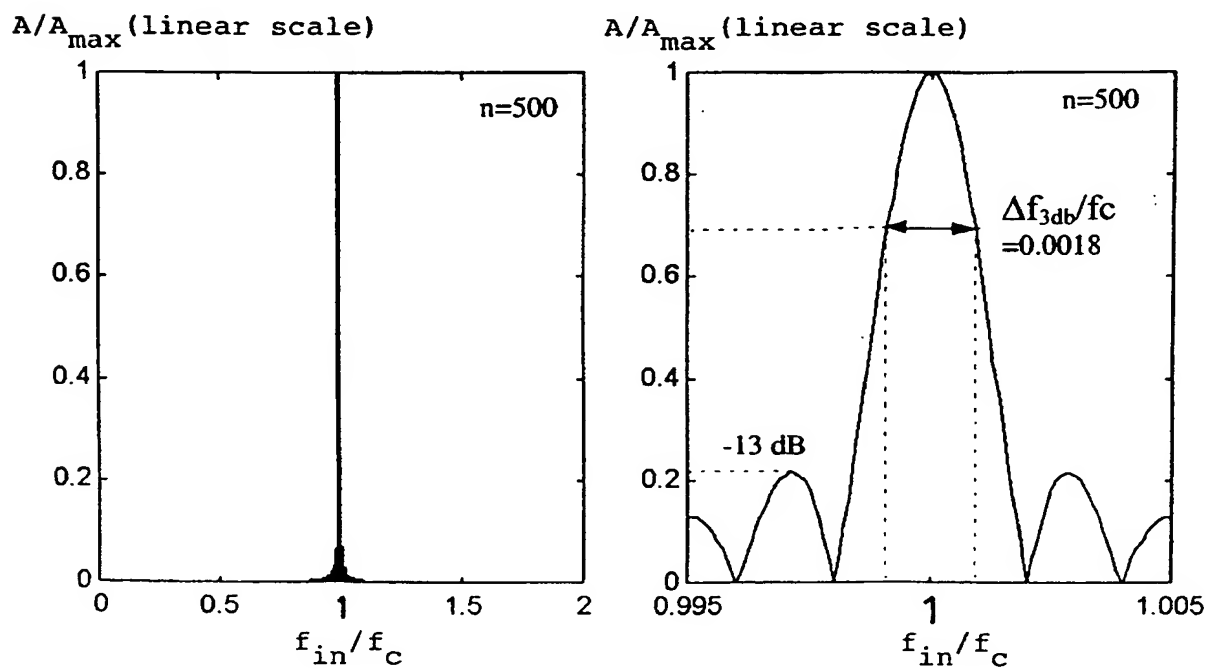
FIG. 7B
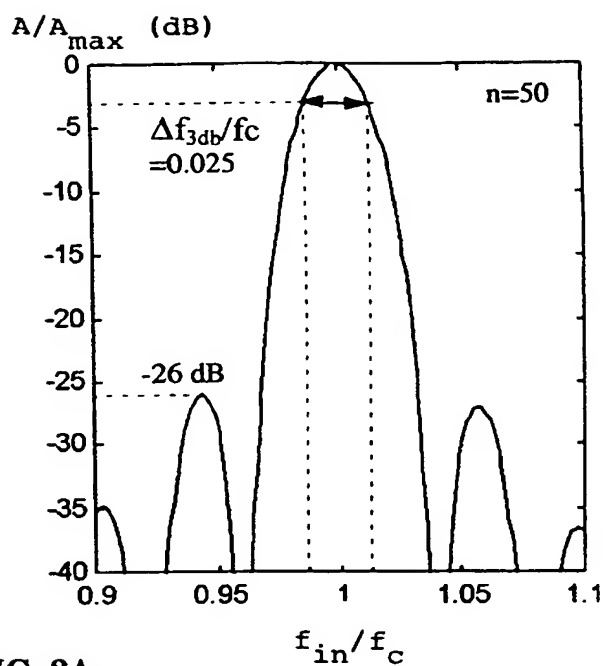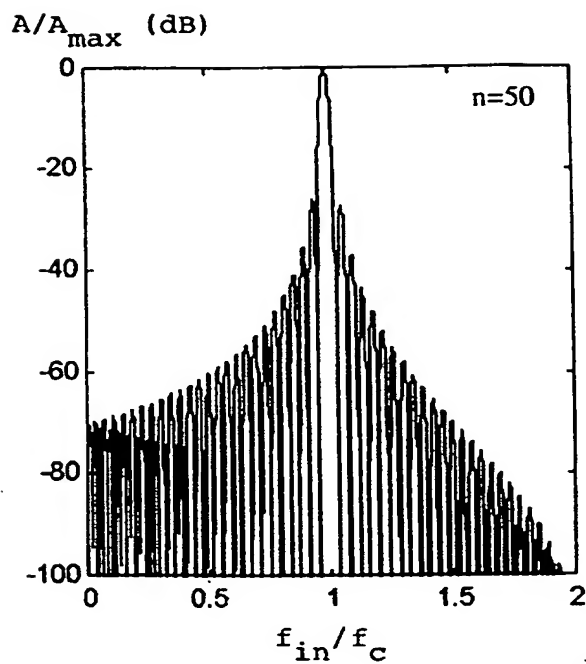
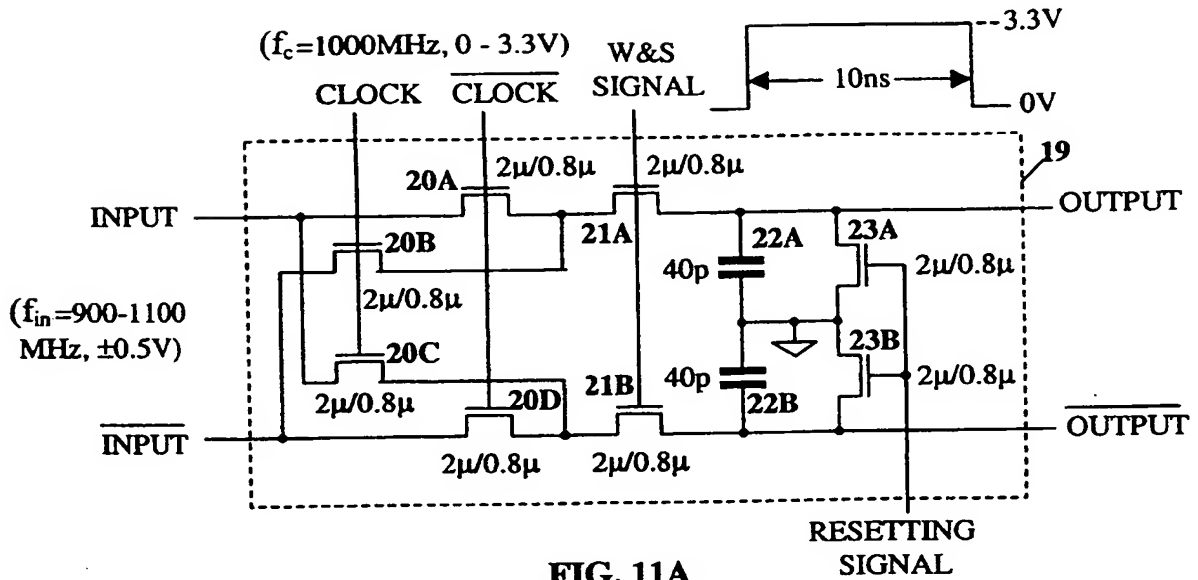**FIG. 8A**
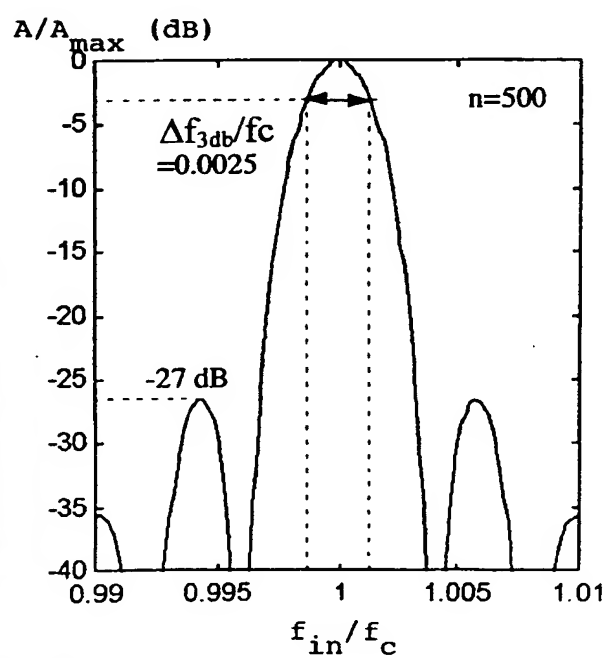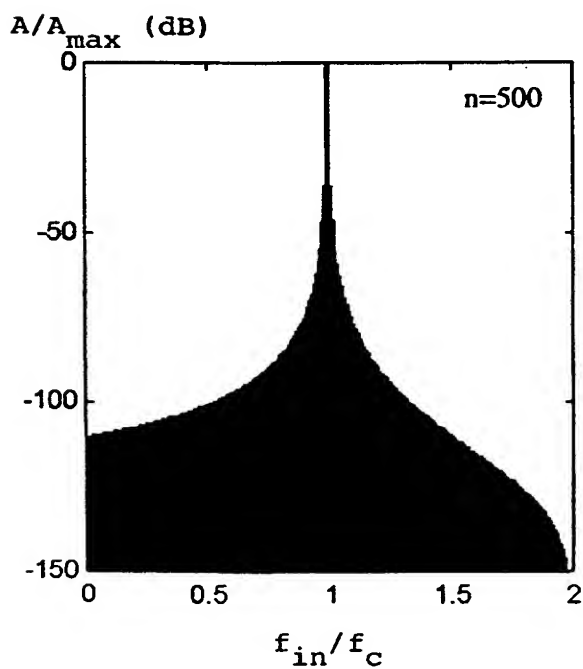
FIG. 8B
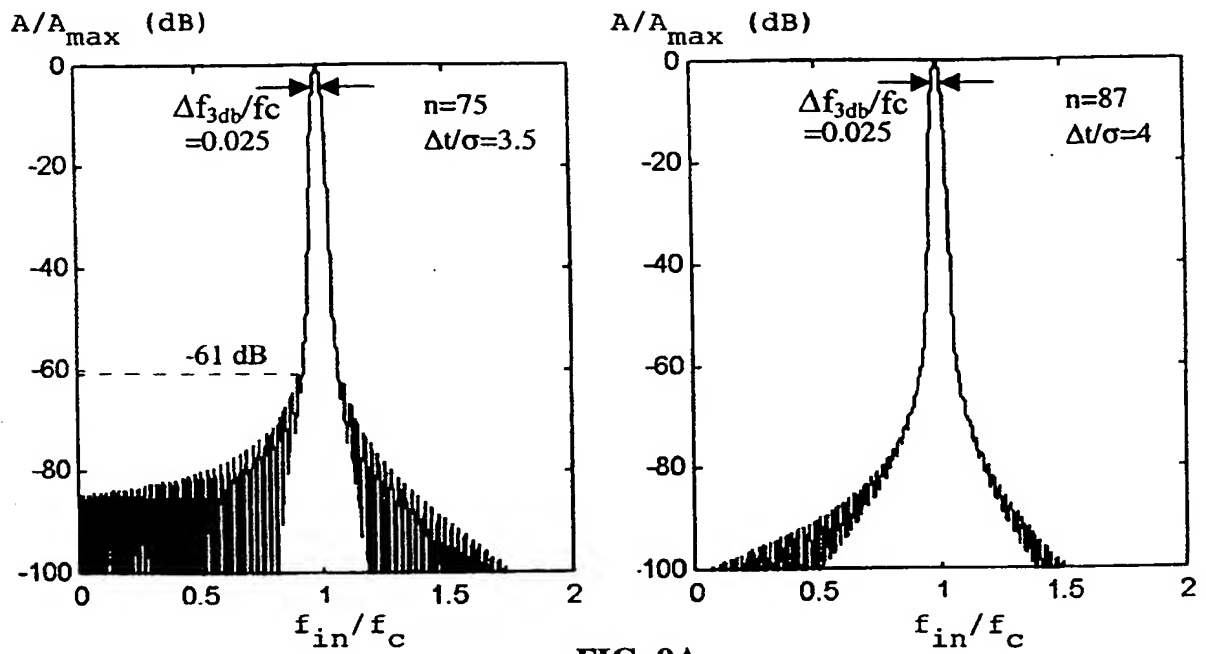
FIG. 9A
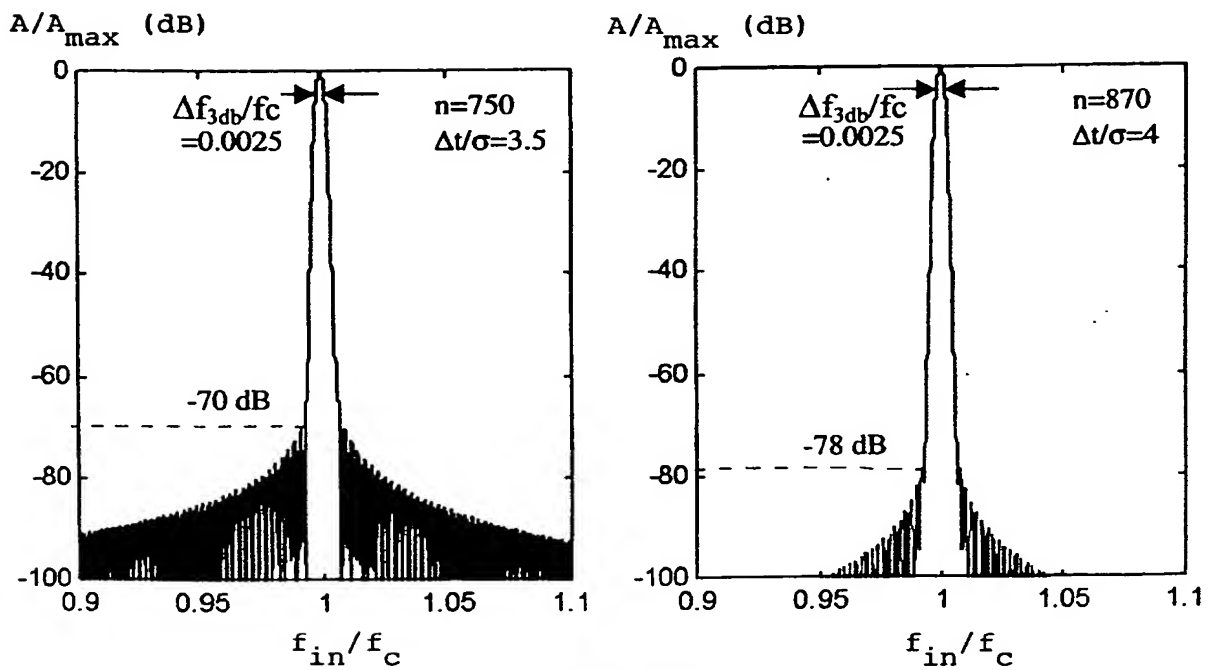
FIG. 9B
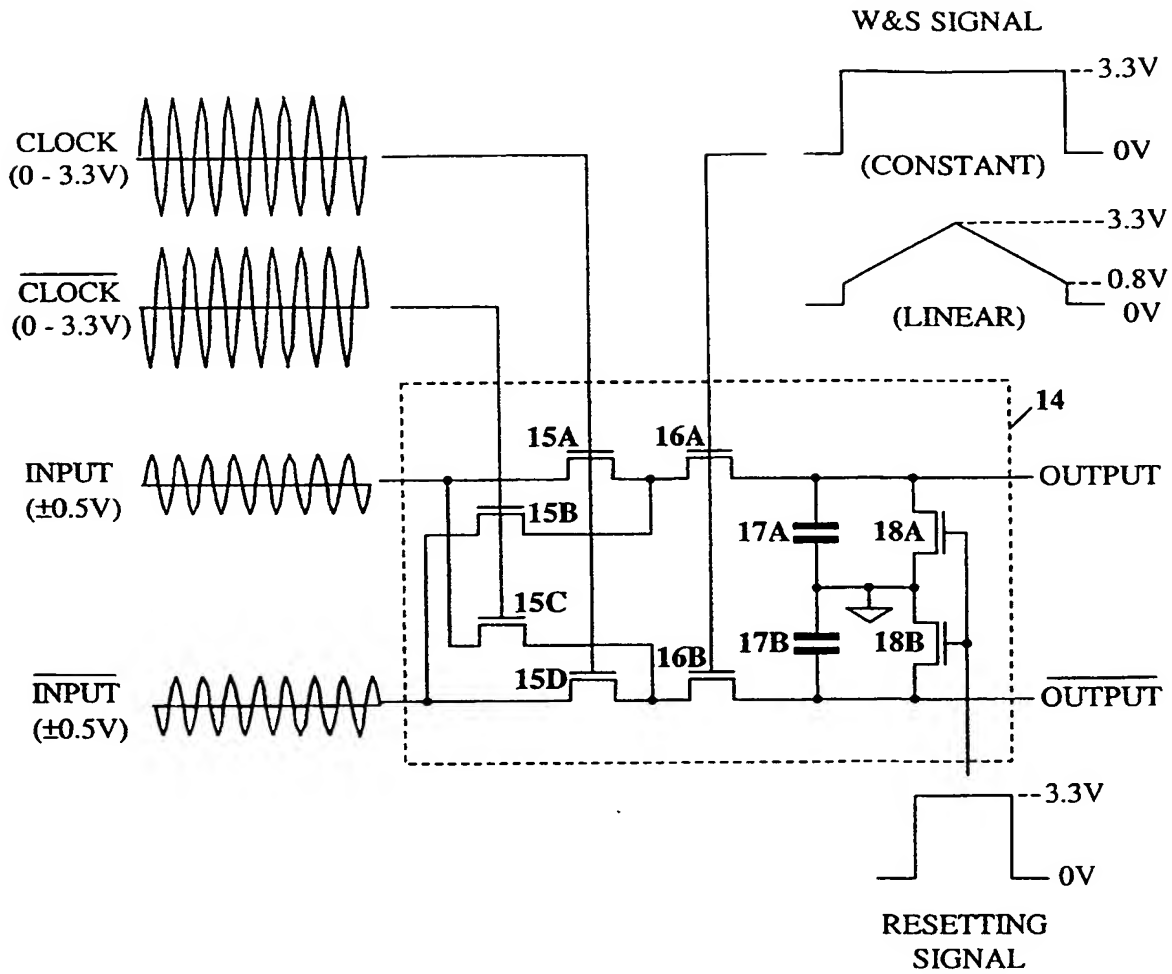
FIG. 10

FIG. 11A

Note: 1. Ideal curve in solid line.
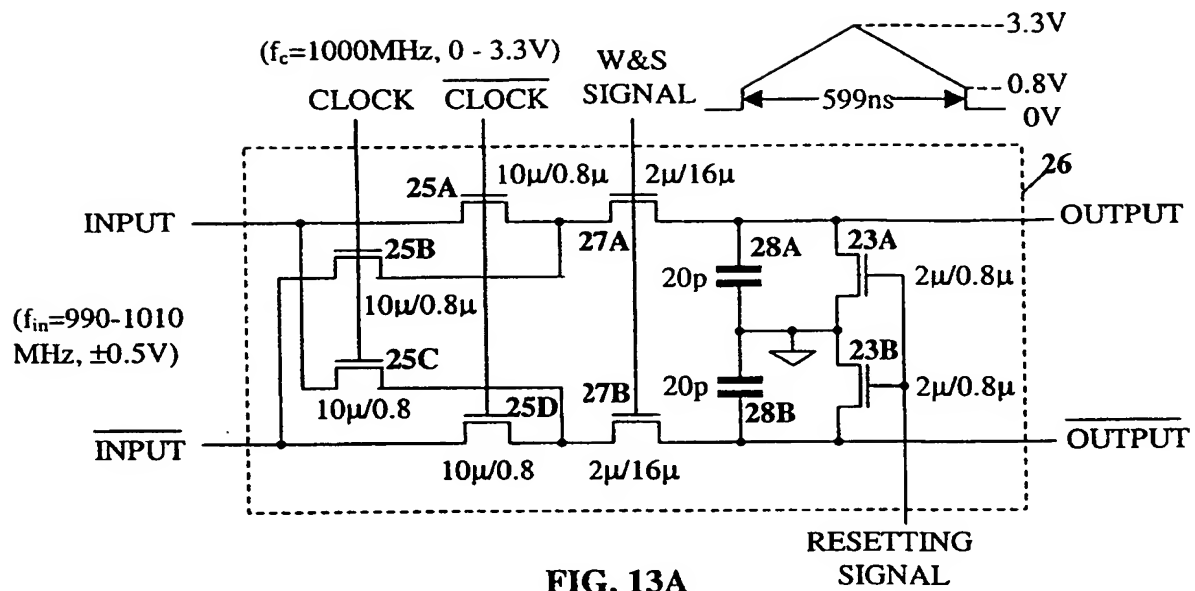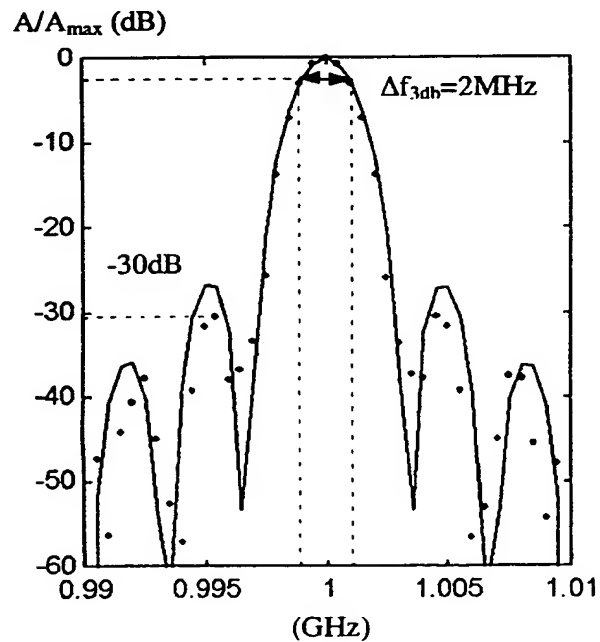2. HSPICE simulation in dots.

FIG. 11B

(f_c=1000MHz, 0 - 3.3V)

CLOCK $\overline{\text{CLOCK}}$

W&S
SIGNAL

3.3V

0.8V

59ns

0V

INPUT

25A 10μ/0.8μ 2μ/0.8μ

24

OUTPUT

25B 21A

22A 23A

40p 2μ/0.8μ

(f_in=900-1100
MHz, ±0.5V)

10μ/0.8μ

25C

10μ/0.8 25D 21B

23B

40p 2μ/0.8μ

22B

$\overline{\text{INPUT}}$

10μ/0.8 2μ/0.8μ

$\overline{\text{OUTPUT}}$

RESETTING
SIGNAL

FIG. 12A

A/A_max (dB)

0

Δf_{3db}=21MHz

-10

-20

-30dB

-30

-40

-50

-60

0.9   0.95   1   1.05   1.1

(GHz)
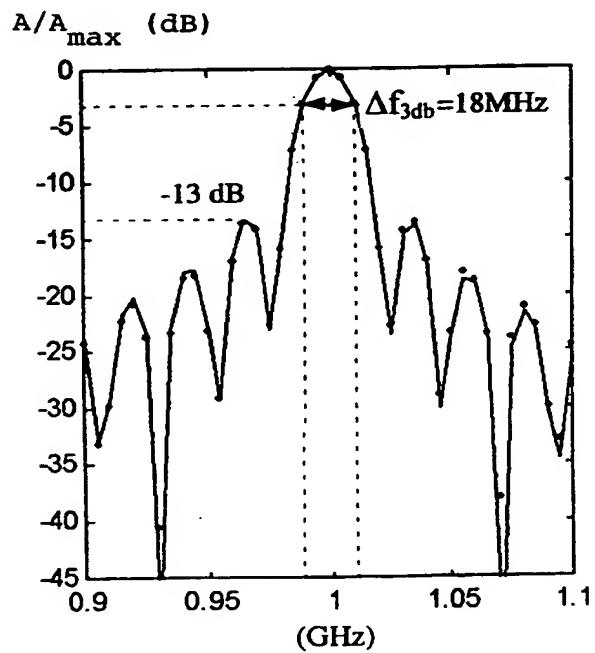
Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 12B

FIG. 13A

Note: 1. Ideal curve in solid line.
2. HSPICE simulation in dots.

FIG. 13B
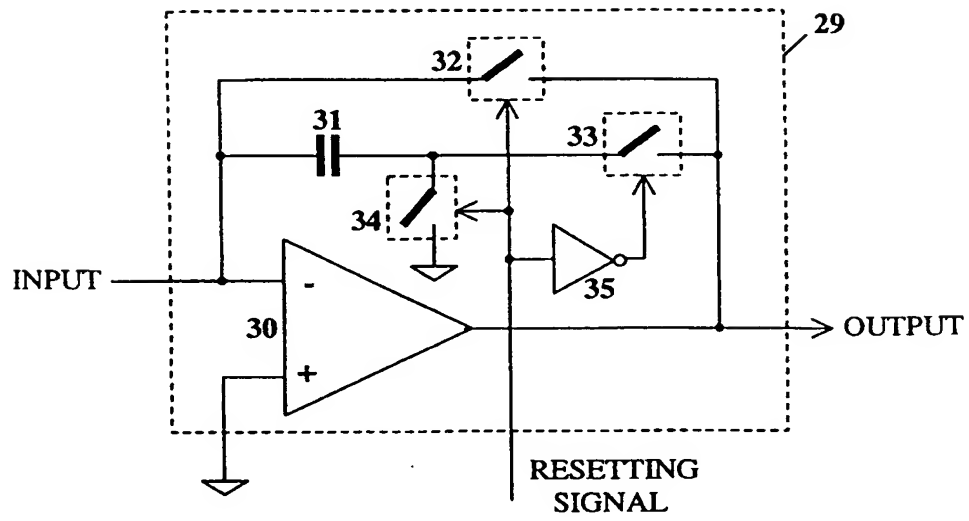
FIG. 14A
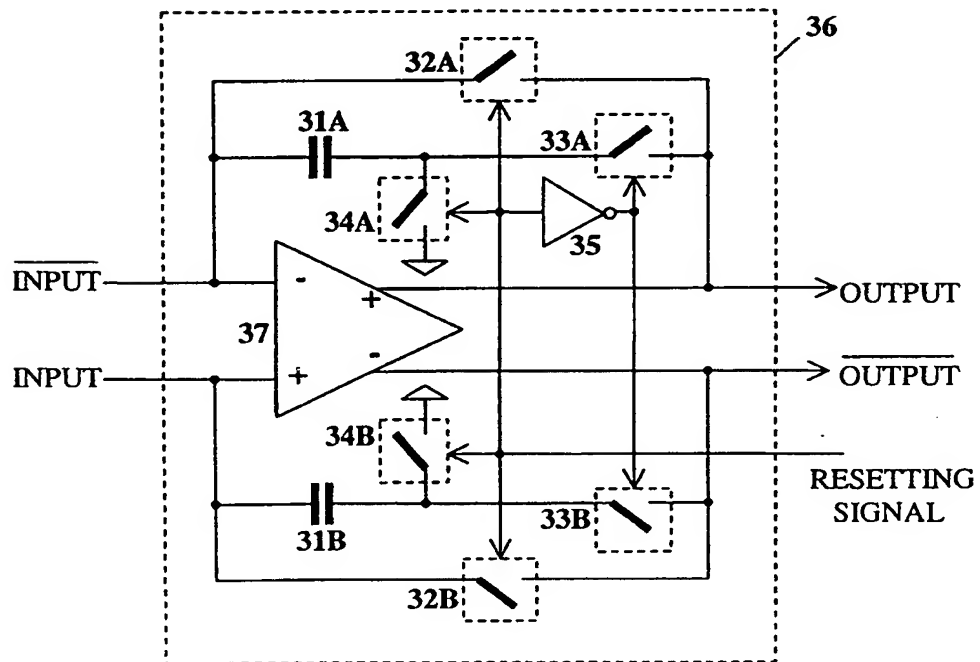

FIG. 14B
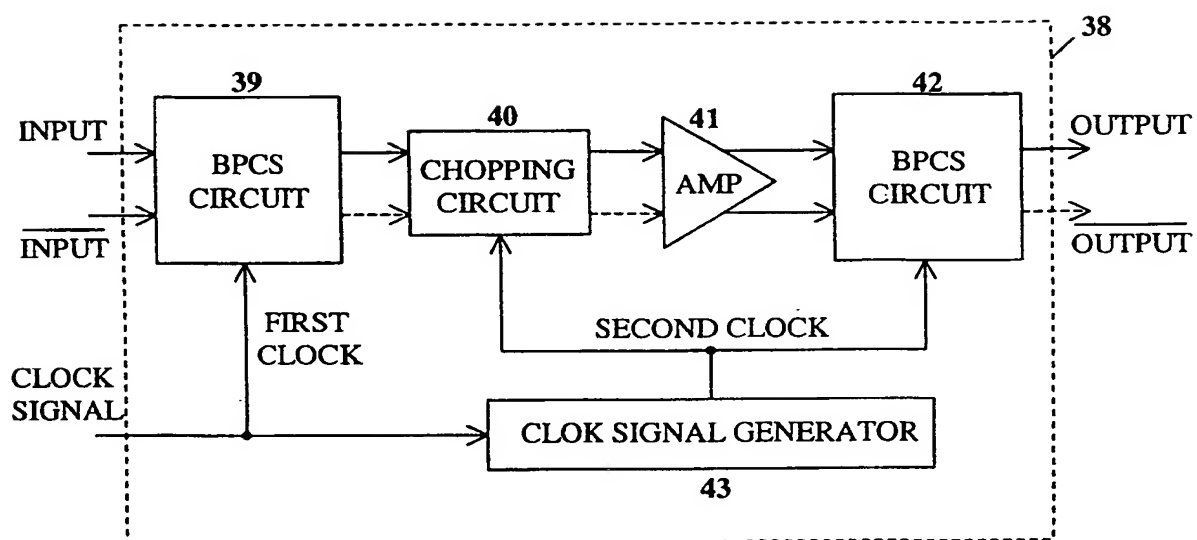
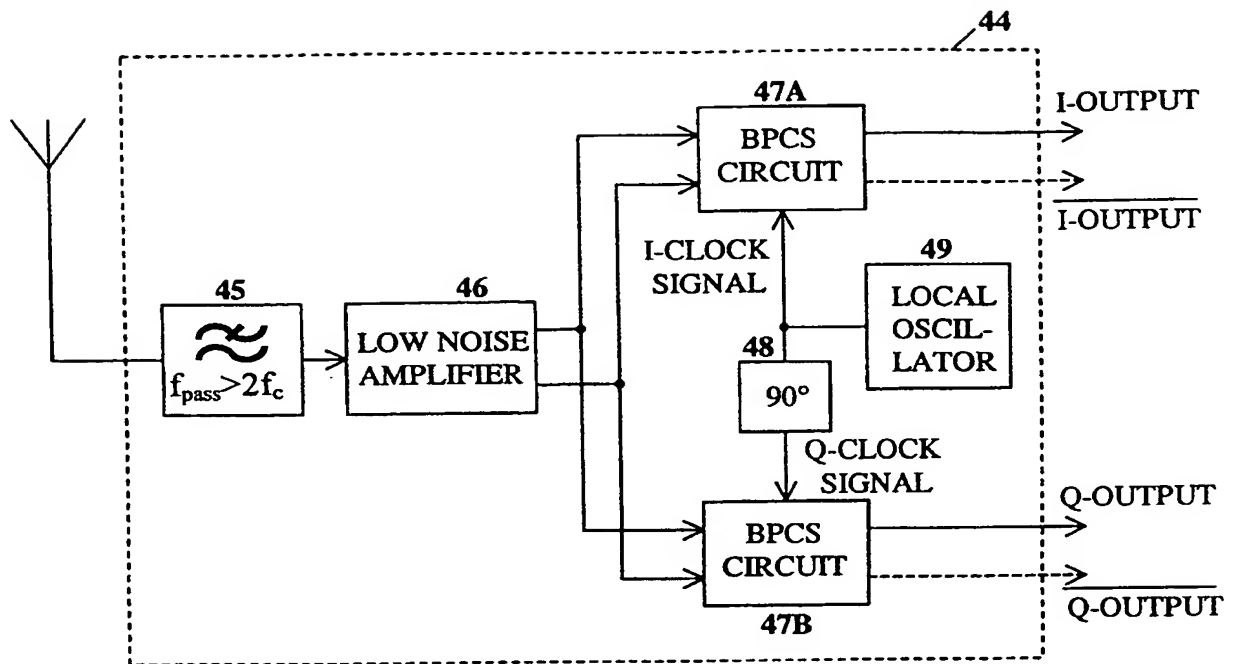FIG. 15

FIG. 16

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G11C 27/02, H03M 1/12, H04B 1/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G11C, H03M, H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5414311 A (L.R. CARLEY), 9 May 1995 (09.05.95), column 3, line 16 – column 4, line 66, figures 4,5	1-3,5,6,28, 30
Y		13-15
	--	
X	US 5698999 A (T. ETOH ET AL.), 16 December 1997 (16.12.97), column 1, line 20 – line 55; column 6, line 39 – column 7, line 26, figures 1,5	1-3,5,6,14, 28,30,31
A		7,9,11,12
	--	

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 2000	2 2 -02- 2001
Name and mailing address of the ISA/	Authorized officer
Swedish Patent Office Box 5055, S-102 42 STOCKHOLM	Bo Gustavsson /OGU
Facsimile No. +46 8 666 02 86	Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1998)

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0741391 A2 (KABUSHIKI KAISHA TOSHIBA), 6 November 1996 (06.11.96), figure 44, abstract	1-3
Y		13,15
	--	
X	WO 9610827 A1 (IMP, INC.), 11 April 1996 (11.04.96), page 4, line 5 - page 5, line 19; page 8, line 27 - page 11, line 31	1-3,5,6,28, 30
	--	
X	JP 10163912 (TOSHIBA CORP) 1998-06-19 (abstract).(online)(retrieved on 2000-12-21). Retrieved from: EPO PAJ Database	1-3,13,15,28
	--	
X	DE 3634637 A1 (SGS MICROELETTRONICA S.P.A.), 30 April 1987 (30.04.87), figure 1	1,2,5,6,28, 30
	--	
X	JP 6236698 (TAMAGAWA SEIKI CO LTD) 1994-08-23 (abstract).(online)(retrieved on 2000-12-21) Retrieved from: EPO PAJ Database	1-3,28
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE00/01854

Box I   **Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
   because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 25
   because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

   See extra sheet

3. ☐ Claims Nos.:
   because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II   **Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

See extra sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: 1-6,13-15,19-24,28-30

Remark on Protest   ☐ The additional search fees were accompanied by the applicant's protest.

                                  ☐ No protest accompanied the payment of additional search fees.

Box I (Observations...)

Claim 25 which, according to the introduction of the claim, relates to arrangements of building blocks of PBCS circuits is drafted in a form making it considerably difficult to arrive at a conclusion as to the scope of the claimed invention. The means contained in the arrangements are listed without clarifying whether these are all part of the arrangements or alternative means for such arrangements. As an example, a "..passive arrangement.." and "active arrangement.." for the integrator are presented in plural versions. Further, the dependency of the claim on other claims is unclear, since it refers to two independent inventions (see box II). Therefore, the claim does not comply with the requirements of Article 17.2(a)(ii)PCT.

Box II (Unity of invention)

The present claims are considered to involve three independent inventions á posteriori (see below). The inventions are described in the following groups of claims:

i) A first invention emanating from claim 4 including claims 5, 6, 13-15, 19-24 and 28-30 relating to a charge sampling circuit, in which the sample values are frequency dependent.

ii) A second invention according to claims 7-12, 16-18 and 31 relating to a charge sampling circuit, wherein the input signals are weighted.

iii) A third invention according to claims 26 and 27 relating to a radio receiver.

The prior-art as described in e.g. US 5414311 A or WO 9610827 A1 show that the technical features appearing in claims 1-3 are well known to the skilled person. Thereby, there are no special technical features as defined in Rule 13.2 in common to the first, second and third inventions as described above. Therefore, unity of invention is lacking in the meaning of PCT Rule 13.1.

Patent document cited in search report			Publication date	Patent family member(s)			Publication date
US	5414311	A	09/05/95	NONE			
US	5698999	A	16/12/97	JP	2708007	B	04/02/98
				JP	8273388	A	18/10/96
EP	0741391	A2	06/11/96	DE	69029933	D,T	14/08/97
				DE	69033468	D,T	03/08/00
				EP	0438927	A,B	31/07/91
				JP	4212794	A	04/08/92
				KR	9402810	B	02/04/94
				US	5162670	A	10/11/92
				US	5343089	A	30/08/94
				US	5376841	A	27/12/94
WO	9610827	A1	11/04/96	AU	3682395	A	26/04/96
				US	5617093	A	01/04/97
DE	3634637	A1	30/04/87	FR	2589266	A,B	30/04/87
				IT	1186340	B	26/11/87
				IT	8522641	D	00/00/00
				US	4746871	A	24/05/88